A Fast Detection Algorithm Suitable for Mitigation of Numerous Power Quality Disturbances

Oscar C. Montero-Hernández, *Member, IEEE*, and Prasad N. Enjeti, *Fellow, IEEE*

***Abstract*—In this paper, a fast detection method for voltage disturbances is explored. The proposed method provides reliable and fast detection for either single-phase or polyphase voltage disturbances such as voltage sags, voltage swells, flicker, frequency change in the utility voltage, and harmonic distortion. The algorithm is based on the theory that allows a set of three-phase voltages be represented as dc voltages in a *d–q* synchronous rotating frame. In this case, the utility input voltages are sensed and then converted to dc quantities in the *d–q* reference frame. Thus, any disturbance at the utility input voltages will be promptly reflected as disturbances in the *d–q* values. Further processing of the signals minimizes the point-on-wave effect and yields a trip signal indicating if the disturbance is a voltage sag or a voltage swell. Analysis, simulation, and experimental results are presented for a three-phase system. The proposed algorithm is implemented on a digital signal processor (DSP)-based system to provide ride-through for critical loads.**

***Index Terms*— Disturbances detection, disturbances mitigation and voltage disturbances, power quality.**

I. INTRODUCTION

A COMMON characteristic of most electronic loads is that they are sensitive to voltage variations. Computers and other sensitive loads can lower their performance or even shutdown the process they are in control due to those variations. Voltage variations can be classified as disturbances that produce voltages below the nominal value, which are called voltage sags, and disturbances that produce voltages above the nominal value, which are called voltage swells. The Information Technology Industry Council (ITIC) has published a curve showing a voltage envelope that can be tolerated by most information technology equipment [1]. This curve is a reference widely used to define when the supply of equipment needs to be compensated due to whether a voltage sag or a voltage swell.

On every existing approach to compensate for voltage disturbances, the very first step is to detect the disturbance itself, then other actions will come such as compensation or disconnection. The importance of the detection stage is critical for applications like static transfer switches (STS) and uninterruptible power supplies (UPS), or approaches where the utility supply must be disconnected as part of the compensation [2], [3].

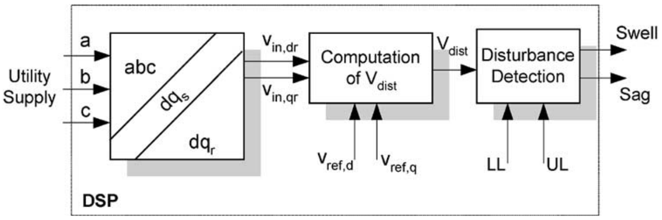

Fig. 1. Block diagram of the proposed approach.

Several ideas have been reported on detection and compensation of voltage disturbances. Some of those works are based on the conversion of the ac voltages of the utility supply to a dc voltage obtained from a rectifier–filter arrange. Any disturbance in the ac supply will be reflected as a change in the dc level; moreover, if the disturbance is unbalanced, some ripple will accompany the change in the level. Additional stages are required to convert this change in the dc level to a useful signal that can generate a signal indicating the existence of a voltage disturbance. One important advantage of this method is its simplicity, but its main drawback is the delay imposed by the filtering stage.

Another popular idea [4]–[9] is based on the *abc–dq* transformation, which in turn gives ac quantities that reflect voltage disturbances on the utility supply. Further processing of those ac signals provides dc signals that are easier to process. One huge advantage of this method is that there are no delays in the process described above. In addition, variations on this method are possible in order to address specific issues such as disturbance magnitude or any phase angle change that the disturbance may introduce [8], [9]. This paper presents a detection method based on the *abc–dq* transformation with an additional processing that minimizes the effect of point-on-wave resulting in a fast detection method. In addition, the method is able to recognize voltage sags and voltage swells as well.

II. PROPOSED APPROACH

Fig. 1 shows the block diagram of the proposed approach. The control circuit is based on a TMS320F240 digital signal processor (DSP), which continuously monitors the source voltages to detect for disturbances. The purpose of the control algorithm is to detect out of tolerance conditions and issue a

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trip signal to enable subsequent actions such as compensation or disconnection.

The algorithm is based on the theory that allows a set of three-phase voltages to be represented as dc voltages in a *d–q* synchronous rotating frame. In this case, the utility input voltages are sensed and then converted to dc quantities in the *d–q* reference frame. Thus, any disturbance at the utility input voltages will be reflected as disturbances in the *d–q* values. Using the disturbed *d–q* values, it is possible to generate the signal called V_{dist}, which represents the deviation of the utility input voltages from a given reference. V_{dist} is used to detect the time when the disturbance begins and when it ends, providing a proper signal to indicate whether the disturbance is a voltage sag or a voltage swell.

III. DISTURBANCE DETECTION ALGORITHM

The disturbance detection algorithm must achieve two important functions to ensure proper operation.

1) Regardless of the nature of the voltage disturbance (sag or swell, either balanced or unbalanced), the algorithm should be able to detect the disturbance immediately. The faster the disturbance is detected, the faster is the application of subsequent actions.
2) It should be able to recognize when the amount of voltage disturbance is beyond certain limits and then deliver a trip signal, otherwise consider the system operating under normal conditions. As an example, sags and swells of 2% or 3% should not be considered conditions out of tolerance.

The first step in the detection algorithm is to convert the set of input voltages from abc to a dq stationary frame, then to a dq synchronous rotating frame where all line frequency components are removed yielding only dc values for the dq variables. This double conversion is achieved by using the expressions

$$\begin{bmatrix} V_{\text{in},ds} \\ V_{\text{in},qs} \\ V_{\text{in},0} \end{bmatrix} = \frac{2}{3} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & -\frac{\sqrt{3}}{2} & \frac{\sqrt{3}}{2} \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} \tag{1}$$

and

$$\begin{bmatrix} V_{\text{in},dr} \\ V_{\text{in},qr} \end{bmatrix} = \begin{bmatrix} \cos\omega t & -\sin\omega t \\ \cos\omega t & \sin\omega t \end{bmatrix} \begin{bmatrix} V_{\text{in},ds} \\ V_{\text{in},qs} \end{bmatrix}. \tag{2}$$

Next, to obtain V_{dist}, a set of three-phase balanced voltages was used as reference, which in turn represents an always-constant dc value in *d–q* synchronous rotating frame. The dc values obtained from (2) are compared against the given reference values as

$$V_{\text{err},dr} = V_{\text{ref},dr} - V_{\text{in},dr} \tag{3}$$

$$V_{\text{err},qr} = V_{\text{ref},qr} - V_{\text{in},qr}. \tag{4}$$

Results from this comparison yield values in *d–q* components of the difference between the reference values and the sensed values from the utility supply. Analysis of the waveforms, obtained from (3) and (4), indicates that the signal containing the information about the deviation of the instantaneous voltage is (4); furthermore, voltage sags and voltage swells are identified from the polarity of this signal. From this analysis, (5) is obtained as

$$V_{\text{dist}} = V_{\text{err},qr} \tag{5}$$

where V_{dist} is the magnitude of the vector that represents the instantaneous deviation of utility input voltages with respect to the given reference. What is not accounted for, until this point, is any phase shift associated with the voltage disturbance. If necessary, however, further processing of the information available from (2) can provide such information. Fig. 2 shows different values of V_{dist} for different conditions on the input utility voltages. In all cases, the upper trace represents 120-V phase voltages from the three-phase utility supply and the lower trace is the waveform associated with V_{dist} as a percentage of the disturbance.

At normal conditions, the *d–q* values obtained from (2) should be equal to the given reference values, when this condition is met, the value of V_{dist} is zero, otherwise V_{dist} is a dc signal varying according to the nature of the disturbance as is shown in Fig. 2.

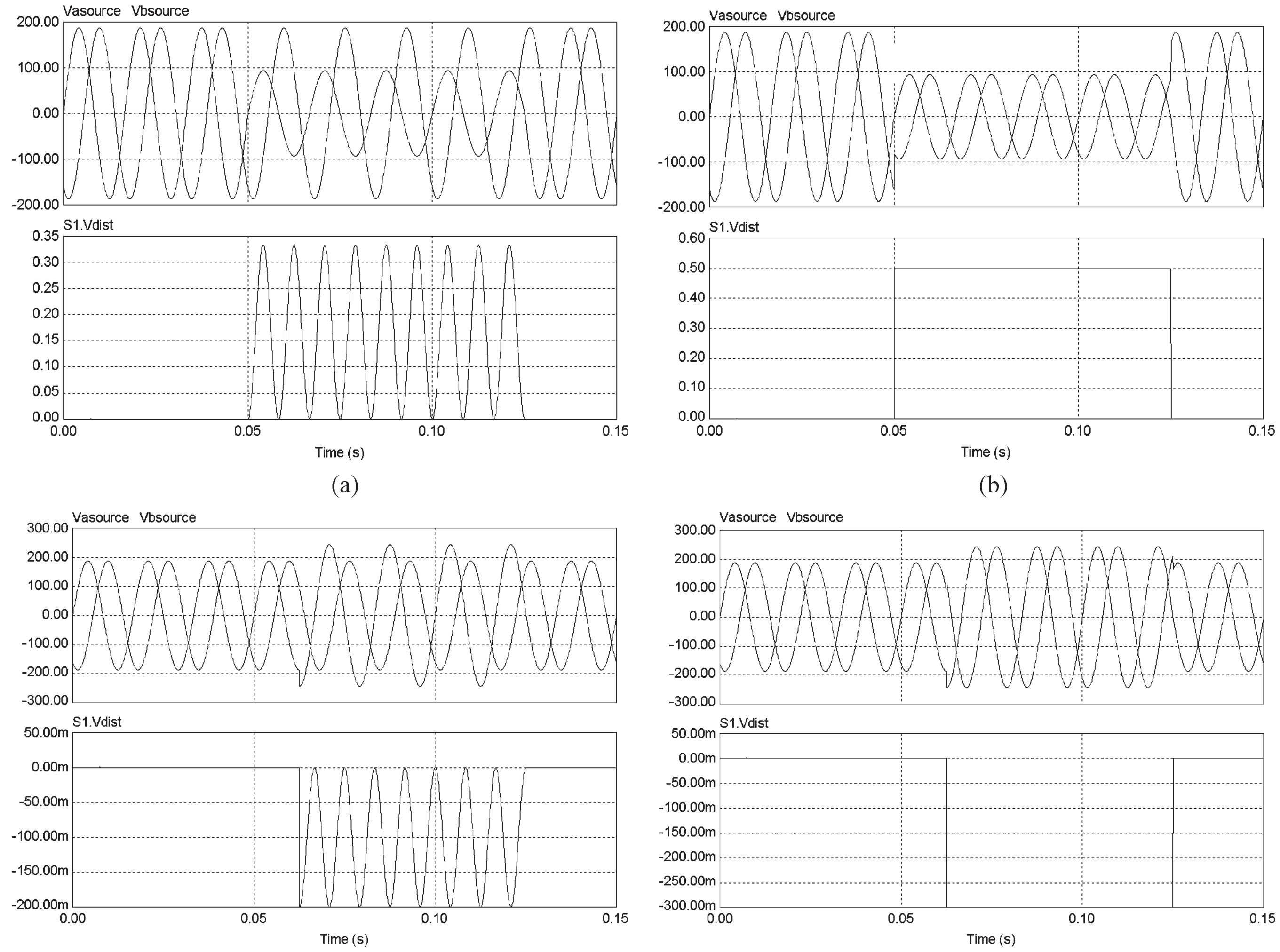
Since V_{dist} is a signal that indicates when a voltage disturbance is present, it is digitally filtered and then processed by a dual hysteresis comparator to produce an ON–OFF signal that indicates the duration and type of disturbance as is shown in Fig. 3. Filtering and comparison are performed by the DSP system already mentioned.

V_{dist} is smoothed by the low pass filter to avoid excessive ripple. This is especially important for single-phase disturbances. The lower and upper limits (LL and UL, respectively) of the hysteresis comparator determine the operating points of the detector. The LL for the sag's comparator is associated with the less severe level of disturbance allowed, which is usually set to 90% of the nominal voltage. UL is set 5% apart from LL to avoid oscillations. It is important to notice that a voltage sag higher than 90% is not considered a sag but a condition within tolerance around rated values. On the other hand, a voltage reduction below 10% is considered as an interruption [10]. Likewise, the swell's compartor LL is set for 110% of nominal voltage. Experimental results for a single-phase sag and a three-phase swell are shown in Fig. 4, where the upper trace is one line voltage from the utility supply, the second trace is the waveform corresponding to V_{dist}, the third trace is the output of the low pass filter, and the lower trace is the trip signal corresponding to a sag and a swell, respectively.

At this point, it is clear that the point-on wave effect is minimized by the combination of the filter and the settings of LL and UL values. This means that the algorithm does not have to wait until the maximum level of disturbance is reached [6].

IV. ALGORITHM EVALUATION: VOLTAGE SAGS CASE

Detection of voltage disturbances can be difficult due to the wide variety of possible cases, for instance, a voltage sag can be a disturbance happening in one, two, or three phases at



(a) (b) (c) (d)

Fig. 2. Relationship between the utility input voltages and V_{dist}. (a) 50% single-phase sag. (b) 50% three-phase sag. (c) 30% single-phase swell. (d) 30% three-phase swell.

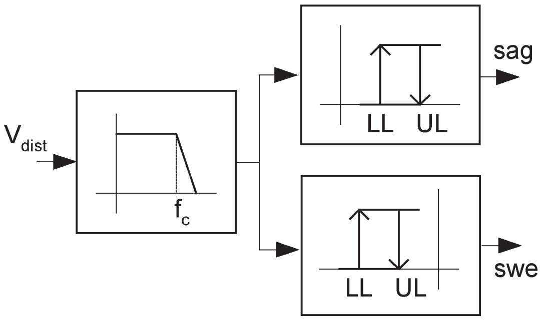


Fig. 3. Processing of V_{dist} in order to obtain a trip signal.

the same time. In order to be considered as significant, such disturbance would have a magnitude ranging from 10% to 90% as explained previously. Moreover, it can occur at any time (point-on-wave) during the 16.6-ms cycle duration [10]. All the factors mentioned before introduce uncertainty and make it difficult to generalize an algorithm for voltage disturbance detection.

A. *Influence of Disturbance Magnitude*

In this particular case, the signal used to detect the onset of disturbance is V_{dist}. According to Fig. 2, V_{dist} will be a pure dc voltage when a three-phase disturbance occurs. It will be a dc voltage with some ripple for a two-phase disturbance (not shown in Fig. 2), and for single-phase disturbances it will be a dc signal oscillating between zero and a maximum value determined by the disturbance magnitude. The voltage magnitude of the disturbance will determine the magnitude of V_{dist} but will not affect its shape. Experimental results for different values of voltage sags are shown in Fig. 5, including the worst scenario about the time required to detect the disturbance as the magnitude of the disturbance is varying. This time is called delay time.

Even though the shape remains unchanged for V_{dist}, its magnitude will influence the delay time. It can be noticed how the response is faster for deeper sags and how single-phase voltage sags are difficult to detect promptly. Slower detection for single-phase sags is due to the highest ripple on the V_{dist} signal compared to other disturbances. During the time the signal is in the valley, the disturbance could be considered as

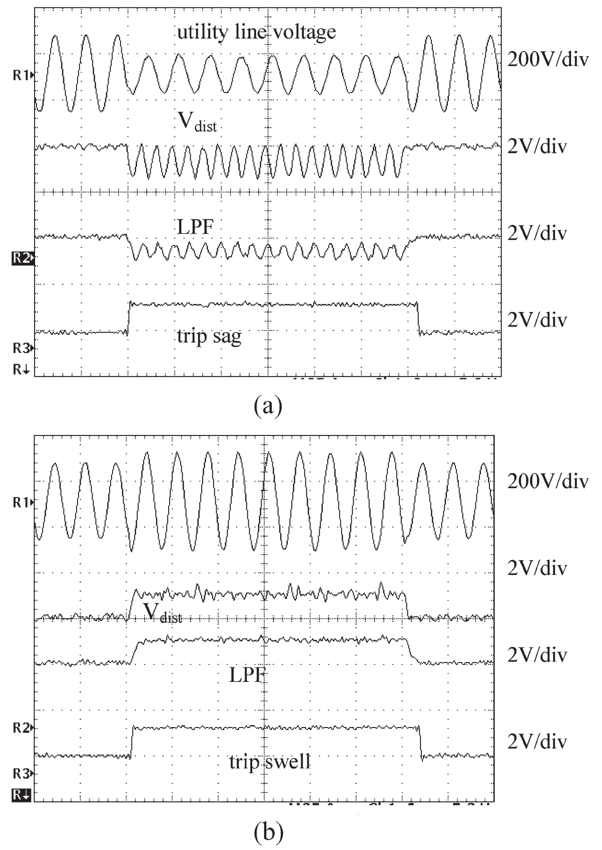


Fig. 4. Experimental results for the detection algorithm. (a) 50% single-phase sag. (b) 30% three-phase swell.

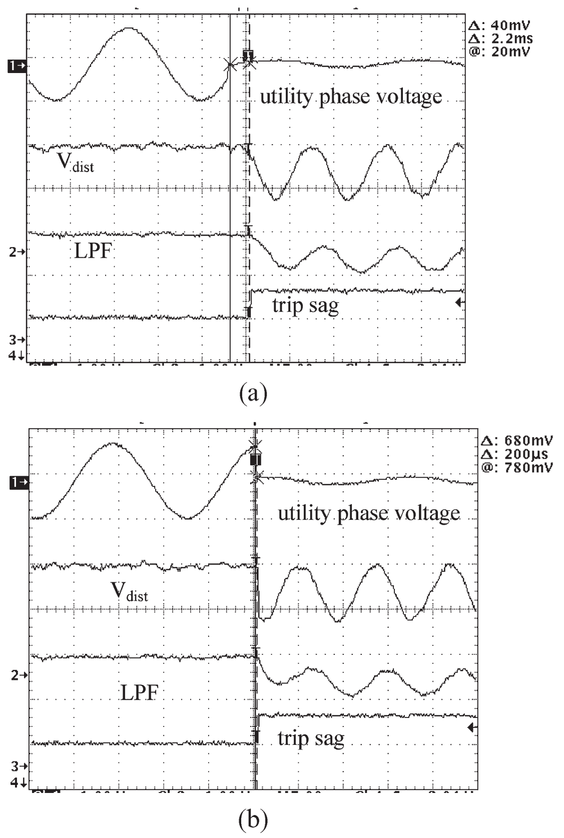


Fig. 6. Effect of point-on-wave effect for single-phase voltage sag of 10%. (a) Worst case. (b) Best case.

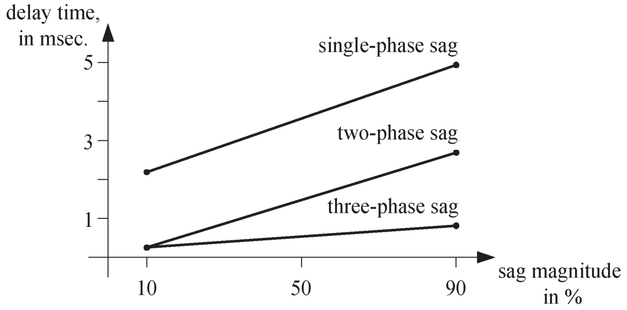


Fig. 5. Experimental results of the delay time as a function of the sag magnitude. Point-on-wave is set constant for the worst case.

negligible and only during the crest of the ripple the disturbance is seen as significant. Therefore, more time is needed to let the detector acknowledge the abnormal condition. The worst case for detecting two-phase and three-phase voltage sags is less than 1/4 cycle.

B. Influence of Point-on-Wave

The point-on-wave is the instant where the disturbance begins. Hence, for a sinusoidal waveform, the point-on-wave is minimum near the zero-crossing area and would be maximum near the peak value of the waveform. The effect of point-on-wave on detection time is further investigated in this section. It should be noted that point-on-wave might have a different impact on the detection time for different detection algorithms.

The point-on-wave time will not affect the initial value of V_{dist} for three-phase disturbances, it will affect V_{dist} mildly for two-phase disturbances, and it will strongly affect the V_{dist} initial value for single-phase disturbances. Based on this reasoning, additional analysis for single-phase voltage sags is presented next.

Fig. 6 shows a single-phase 10% voltage sag for two different point-on-wave times. Fig. 6(a) shows the worst scenario with a time delay of 2.2 ms and Fig. 6(b) shows the best scenario with a time delay of 200 μs.

The upper trace in Fig. 6 corresponds to one phase of the utility supply, the second trace corresponds to V_{dist}, the third trace is the response of the low pass filter, and the bottom trace is the trip signal indicating that a sag has started.

Experimental delay times showing the effect of different point-on-wave values for single-phase voltage sags on the proposed algorithm are summarized in the next figure.

The area described for the polygon in Fig. 7 encompasses all the possible responses of the algorithm under different sag magnitudes at any point-on-wave. The upper line of the polygon is the same as the one described as the worst case for single-phase sags in Fig. 5. It can be noticed that all the voltage sags are detected no matter their magnitude. In addition, the deeper the sag, the faster the response. Despite the wide variation in

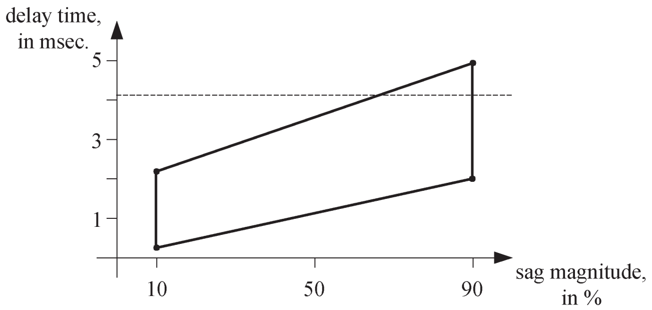


Fig. 7. Effect of point-on-wave over the time delay for single-phase voltage sags.

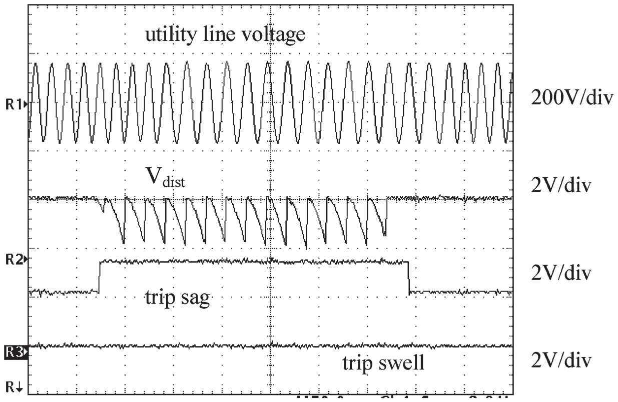


Fig. 8. Experimental results showing the detection of a change in the fundamental frequency from the utility supply.

time of the algorithm response, most of the expected delay times are below 1/4 cycle. For two-phase voltage sags, the area defined by the worst case and the best case is much smaller than the area shown in Fig. 7 and the area for three-phase voltage sags is practically inexistent.

V. DISTURBANCES AND TESTING

Additional testing has been performed with the system for disturbances such as frequency change, voltage flicker, and voltage harmonics as is shown in the next figures.

Fig. 8 shows the response of the system under a frequency change. The nominal frequency is 60 Hz and then a change in frequency occurs leading to a trip.

Detection of a voltage flicker is very similar to detection of a voltage sag as is shown in Fig. 9. The voltage is reduced up to 80% of its nominal value in 0.1 s, then the voltage recovers back to its original value in 0.2 s.

For a disturbance such as harmonic distortion, the system will not operate whenever the voltage distortion is low, but if the distortion is high enough it can trigger the hysteresis comparator as is shown in Fig. 10.

In this case, the utility line voltage is distorted by the fifth and seventh harmonics. The result is a trip in the signal called trip sag while the signal called trip swell remains at low state.

Voltage sags, voltage swells, and voltage flicker are disturbances with relative short duration that may have an impact on the load due to significant variations of the nominal voltage.

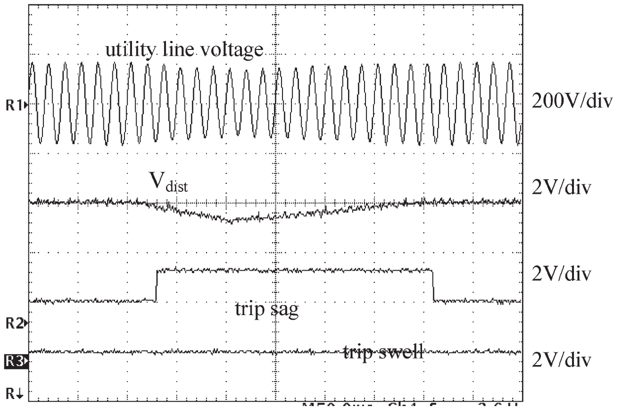


Fig. 9. Experimental results showing the detection of a voltage flicker.

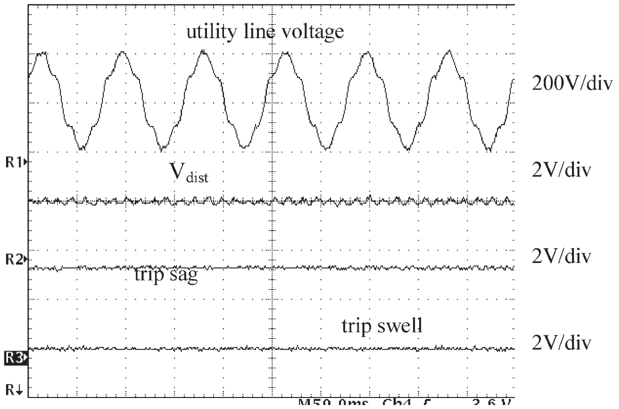


Fig. 10. Experimental results for harmonic distortion detection.

Therefore, settings for LL and UL should be set according to the description presented in Section III. That is, LL and UL are associated with the disturbance voltage level. On the other hand, voltage disturbances such as harmonic distortion may have a different impact on the load. Therefore, LL and UL should be set as the amount of allowed harmonic distortion rather than the distortion voltage level. In this regard, it is recommended to have separate detection systems for voltage disturbances and harmonic distortion with different values of LL and UL, respectively.

For the case of distortion caused by notches, the settings LL and UL in the hysteresis comparators play a very important role. If the settings are defined for high sensitivity, then it is possible that some notches can cause a trip; on the other hand, if the settings are for low sensitivity, then the notches will not be detected as a disturbance but the response of the system to other disturbances, such as voltage sags, could be slow.

VI. RIDE-THROUGH APPROACH FOR CRITICAL LOADS

The proposed algorithm has been implemented in the ride-through approach shown in Fig. 11 [3]. Here, the prompt detection of a voltage disturbance will transfer the load supply from the utility supply to the inverter supply via the proper operation of the solid state switches labeled SSA and SSM.

Fig. 12 shows the experimental results of the detection algorithm when a voltage swell occurs right after a voltage sag. In

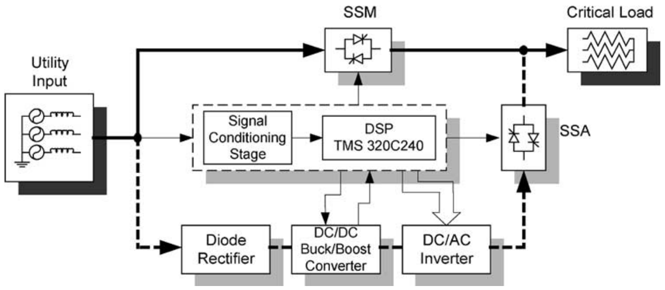
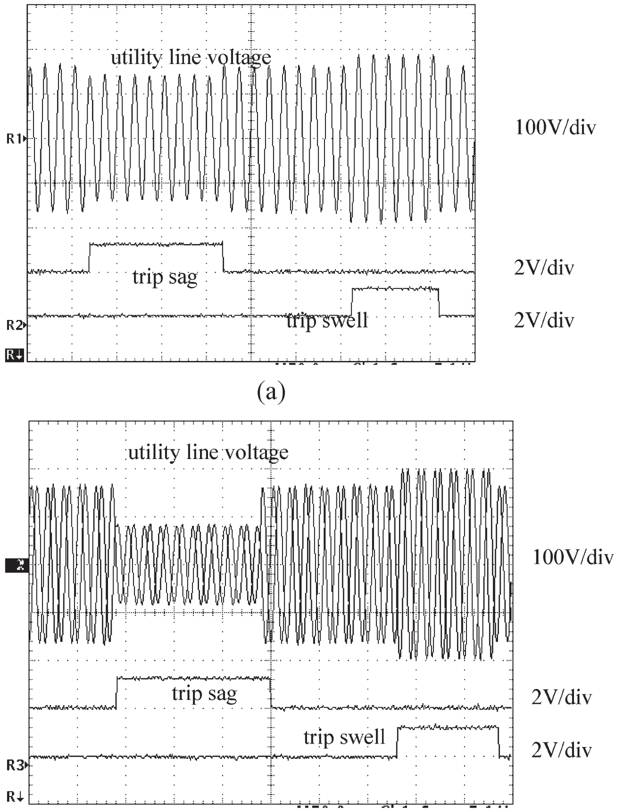


Fig. 11. Ride-through approach.



(a)

(b)

Fig. 12. Experimental results showing the detection of (a) 85% single-phase sag followed by a 115% single-phase swell and (b) 50% three-phase sag followed by a 120% three-phase swell.

both cases, the upper trace corresponds to the utility input line voltages, the trace in the middle represents a trip when a sag occurs, and the lower trace indicates when a swell is present. Notice that a sag trip signal does not occur at the same time of a trip swell signal.

VII. CONCLUSION

Detection of voltage disturbances is the first step in the process to improve voltage quality. Voltage disturbances are difficult to detect due to the extended variety of combinations resulting from the factors involved in voltage disturbances such as magnitude, point-on-wave, balance, and frequency. This diversity makes impossible the generalization of an algorithm, leading to a tradeoff between speed and sensitivity. The proposed algorithm is capable of detecting voltage sags and voltage swells no matter their magnitude as well some other disturbances. In addition, the algorithm guarantees the detection of either balanced or unbalanced voltage disturbances. The detection time of the worst case corresponds to single-phase voltage sags; even in this case, most of the delay time expected is less than 1/4 cycle.

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Dr. Enjeti was elected to Fellow by the IEEE Fellow Committee for "Contributions to solutions of utility interface problems in power electronic systems and harmonic mitigation" in 2000. He was the recipient of the IEEE Industry Applications Society (IAS) Best Paper Award in 1993, 1996, 1998, 1999, and 2003; the Second Best IEEE-IAS Transaction Paper published in mid-year 1994 to mid-year 1995, and IEEE-IAS Magazine Prize Article Award in the year 1996. He was also the recipient of the select title "Class of 2001 Texas A&M University Faculty Fellow" Award for demonstrated achievement of excellence in research, scholarship, and leadership in the field. In 2004, he was named Texas Instruments Professor in Engineering.