

# Analysis of Common Mode Voltage—“Neutral Shift” in Medium Voltage PWM Adjustable Speed Drive (MV-ASD) Systems

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**Abstract**—In this paper analysis of common mode voltage or “neutral shift” in the new emerging voltage source inverter type medium voltage adjustable speed drive (MV-ASD) systems is presented. Both cascaded multilevel (CML) inverter and 3-level NPC inverter topologies are analyzed. An equivalent circuit model to determine the common mode voltage stress is presented. Analysis and simulation results are discussed and worst case common mode voltage excursion is computed for an example 800 Hp, 4160 V MV-ASD. It is shown that certain system components are excessively stressed and in the MV-ASD system these data are particularly useful in specifying system components and for proper design of the system. Possible effects of common mode voltage and its  $dv/dt$  on medium voltage motor bearings are discussed. A new multilevel PWM strategy is introduced which results in zero common-mode voltage. Simulation results are shown to illustrate the effectiveness of these schemes. Finally, experimental results from a 800 hp, 4160 V, MV-ASD system are presented.

**Index Terms**—Common mode, medium voltage drive.

## I. INTRODUCTION

**M**EDIUM voltage adjustable speed drive (MV-ASD) systems offer significant advantages in fan, pump and many process control applications with higher efficiencies combined with energy savings over a wide range of speed settings [1]–[4]. MV-ASD systems continue to grow at a steady rate of 9% and find expanding applications [1]. Commercial MV-ASD systems are both current source inverter (CSI) and voltage source inverter (VSI) type [1]–[10]. The CSI approach employs SCR/GTO devices and the VSI approach consists of two types: 1) cascaded multilevel (CML) inverter topology (Fig. 1) employing low voltage IGBT devices [2]–[4] and 2) 3-level NPC Inverter with IGCT devices [Fig. 9(a)] [9], [10].

It has been shown in CSI based MV-ASD systems that the common mode voltage, often termed as “neutral shift,” can be as high as 2.4 pu of rated phase voltage, thus creating a line to ground voltage approaching 3.3 pu [5], [7]. This being higher

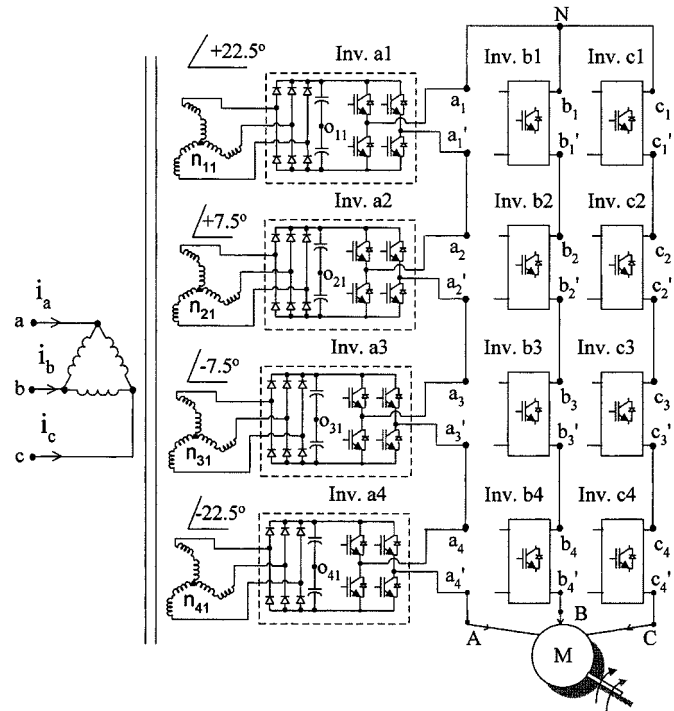


Fig. 1. Example of cascaded multilevel (CML) voltage source inverter for 4160 V, 800 Hp, MV-ASD system. (Note: Input transformer has a total of 12-secondary windings, only four are shown.)

than normal common mode voltage or “neutral shift” has contributed to some motor failures in the field [5], [7].

A brief review of MV-ASD applications suggests that the systems in general, associated with critical process areas of the plant and any shutdown of the system, could result in a major process upset and loss of production [8]. In view of this, the common mode voltage stress or neutral shift in MV-ASD’s is an important issue to consider.

Previous work in this area has focused primarily on CSI based load commutated inverter systems [6], [8]. Voltage source Inverter MV-ASD systems based on 3-level NPC with IGCT devices and CML approach with IGBT’s are presently being introduced into the market place [2], [10]. In view of this, analysis of these new types of MV-ASD systems is therefore timely and is the purpose of this paper.

An equivalent circuit model to determine the common mode voltage is presented. System parameters such as motor/transformer capacitance to ground are experimentally determined on

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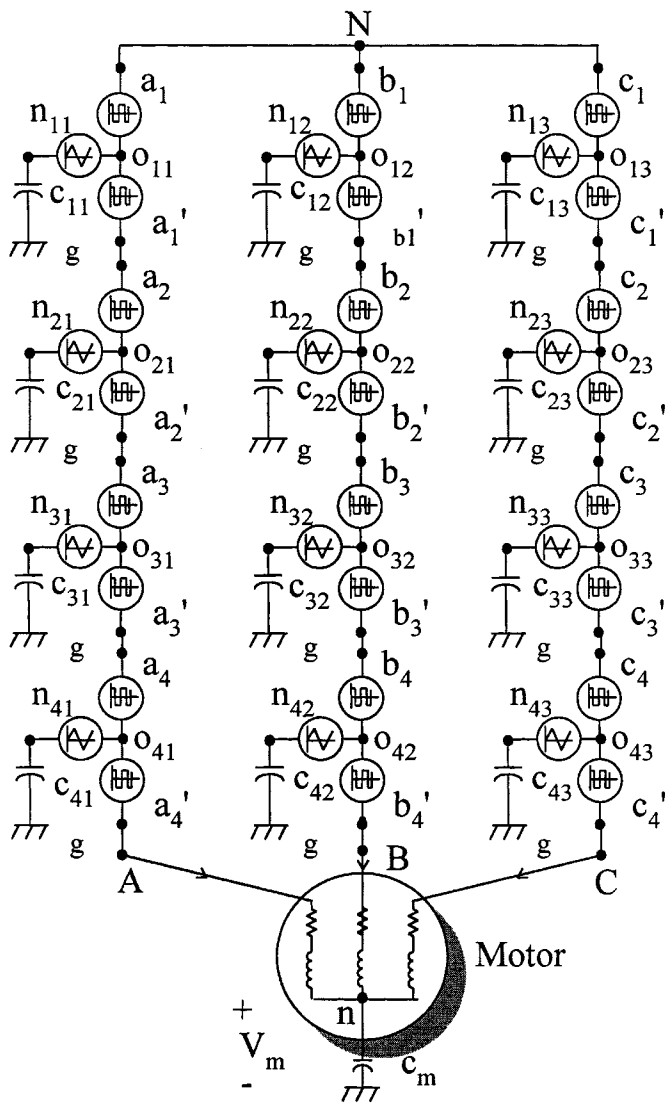


Fig. 2. Equivalent circuit of the CML inverter topology for common-mode voltage analysis.

TABLE I  
COMMON MODE EQUIVALENT CAPACITANCE OF TRANSFORMER SECONDARY WINDINGS IN A MCL-MVD

| Equivalent Cap. | Value  | Equivalent Cap. | Value  |
|-----------------|--------|-----------------|--------|
| C <sub>11</sub> | 395 pF | C <sub>32</sub> | 433 pF |
| C <sub>21</sub> | 420 pF | C <sub>42</sub> | 420 pF |
| C <sub>31</sub> | 425 pF | C <sub>13</sub> | 422 pF |
| C <sub>41</sub> | 413 pF | C <sub>23</sub> | 433 pF |
| C <sub>12</sub> | 417 pF | C <sub>33</sub> | 436 pF |
| C <sub>22</sub> | 430 pF | C <sub>43</sub> | 412 pF |

TABLE II  
COMMON MODE EQUIVALENT CAPACITANCE OF A 4-POLE, 4160 V, 800 hp INDUCTION MOTOR

| Equivalent Cap. | Value    |
|-----------------|----------|
| C <sub>m</sub>  | 65000 pF |

an example of 800 Hp, 4160 V, CML, inverter MV-ASD. Simulation results for varying output frequency are discussed and worst case common mode voltage excursion is computed. It is shown that certain system components are excessively stressed and these data are particularly useful in specifying system com-

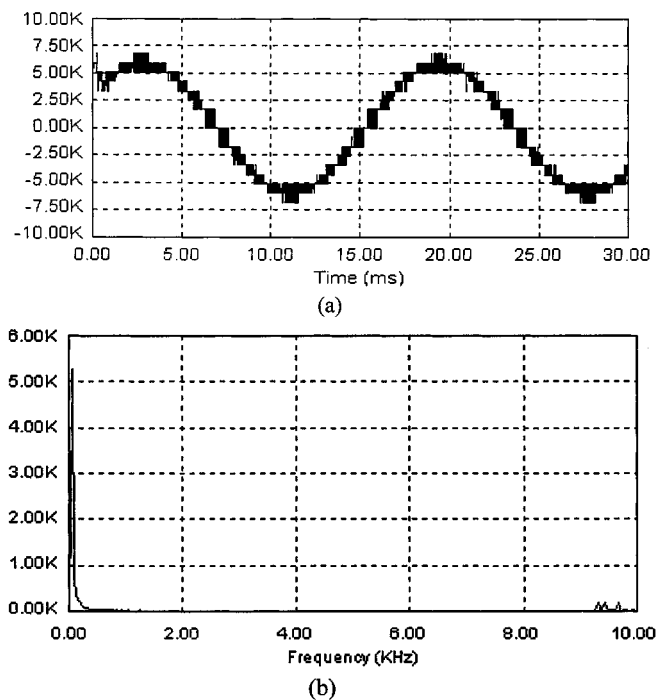


Fig. 3. (a) Voltage (4160 V, rms) across motor terminals for CML MV-ASD topology. (b) The fit of the voltage in Fig. 3(a).

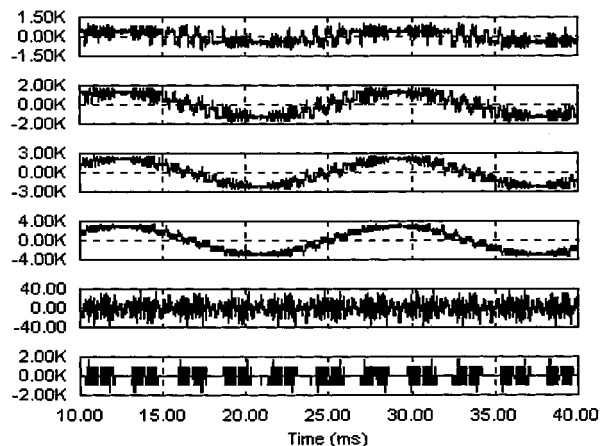


Fig. 4. Voltage potential between neutral points to ground of the phase-a transformer secondaries in the CML inverter topology (see Fig. 2). From top to bottom: voltages  $V_{n_{11},g}$ ,  $V_{n_{21},g}$ ,  $V_{n_{31},g}$ ,  $V_{n_{41},g}$ ,  $V_m$ , and  $3V_{CM}$ .

ponents and for proper design of the system. Possible effects of common mode voltage on medium voltage motor bearings are discussed. Several methods to reduce the common mode voltage stress on the motor in new and retrofit MV-ASD systems are shown.

## II. COMMON MODE VOLTAGE IN CML, MV-ASD SYSTEMS

In this section, analysis of common-mode voltage in CML, MV-ASD systems is presented. Analysis for the NPC based medium voltage ASD systems is provided in Section III.

### A. CML, MV-ASD System

Fig. 1 shows the general topology of a commercially available CML Inverter for MV-ASD's [2]. Several single-phase in-

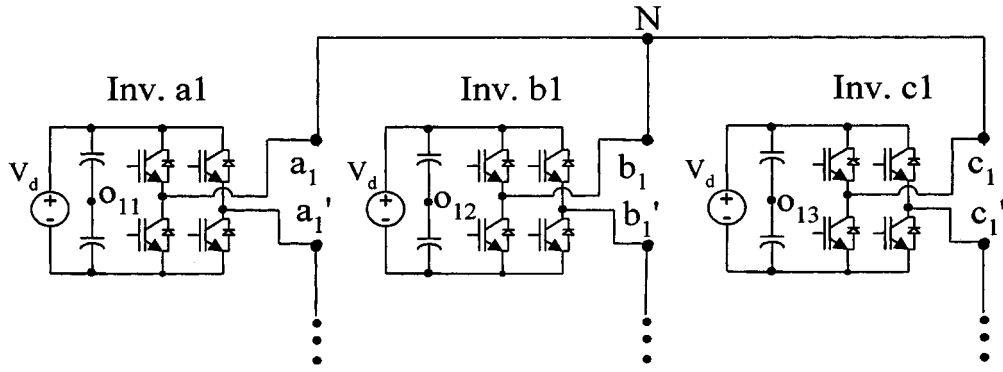


Fig. 5. Stage-I topology of the CML inverter shown in Fig. 1.

verter cells are connected in series in each phase. An input isolation transformer with multiple secondary windings powers each inverter cell via a rectifier and a dc-link. The transformer secondary windings are suitably phase-shifted to realize a multipulse system, which exhibits “clean” input power characteristics. An example 4160 V (line to line) CML inverter consists of an input transformer with 12-secondary three-phase windings and 12 inverter cells (four in each phase), each rated for 600 V (rms) output. A centralized PWM controller operates each inverter cell in a synchronous manner suitably phase shifting the PWM carrier signals to achieve multistep PWM output (Fig. 3). The overall CML inverter output is of high quality over a wide range of output frequency.

### B. Common Mode Equivalent Circuit of CML-MV ASD

Fig. 2 shows the equivalent circuit of the CML Inverter MV-ASD systems suitable for common mode voltage or “neutral shift” analysis. The equivalent circuit can be derived from the CML inverter topology (Fig. 1) as follows: The nodes  $o_{11}, o_{21}, o_{31}, o_{41}$  constitute the dc-link mid points of four single-phase inverter cells in phase-A. Further,  $C_{11}$  to  $C_{41}$  represent the equivalent capacitances between ground and the input transformer secondary windings connected to each single-phase inverter in phase-A. The voltage  $V_{o_{11}, n_{11}}$  represents the voltage between the dc-link midpoint  $o_{11}$  and the secondary winding neutral point  $n_{11}$  as shown. Also  $V_{a_1, a'_1}$  to  $V_{a_4, a'_4}$  represent the PWM output voltages of single-phase inverter cells 1 to 4 in phase-A respectively. Further,  $C_m$  represents the equivalent motor winding capacitance to ground. Tables I and II in Appendix A show the measured values of all the capacitances with respect to ground on a 800 hp, 4160 inverter/motor drive system. It is clear from Tables I and II that the motor winding capacitance  $C_m$  to ground is much larger (nearly 150 times) than the transformer secondary winding capacitances to ground. Further, the transformer secondary winding capacitances to ground for 12 secondaries are nearly equal.

From the equivalent circuit shown in Fig. 2 various voltages with respect to ground can be determined via simulation. From Fig. 2 it can be seen that

$$V_{AN} = V_{a'_1, a_1} + V_{a'_2, a_2} + V_{a'_3, a_3} + V_{a'_4, a_4}. \quad (1)$$

Similarly  $V_{BN}$  and  $V_{CN}$  are given by

$$V_{BN} = V_{b'_1, b_1} + V_{b'_2, b_2} + V_{b'_3, b_3} + V_{b'_4, b_4} \quad (2)$$

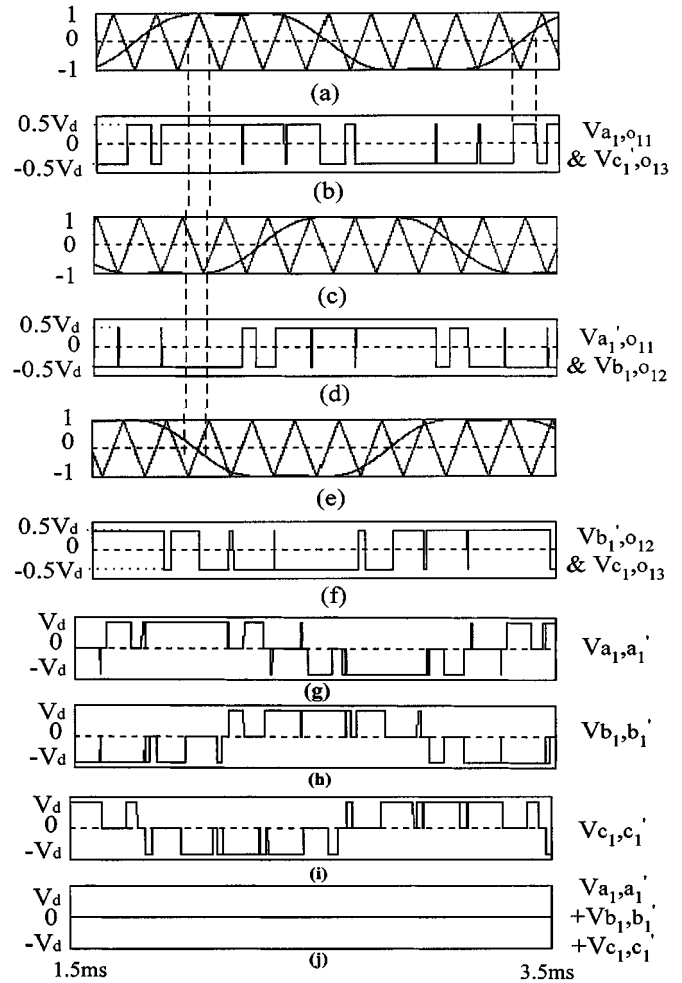


Fig. 6. Example waveform for the proposed common mode cancellation strategy.

$$V_{CN} = V_{c'_1, c_1} + V_{c'_2, c_2} + V_{c'_3, c_3} + V_{c'_4, c_4}. \quad (3)$$

The common mode voltage generated by the cascaded inverter modules is given by

$$V_{CM} = \frac{V_{AN} + V_{BN} + V_{CN}}{3}. \quad (4)$$

The instantaneous summation of PWM voltages  $V_{AN} + V_{BN} + V_{CN}$  may not be zero and is dependent on the PWM strategy employed.

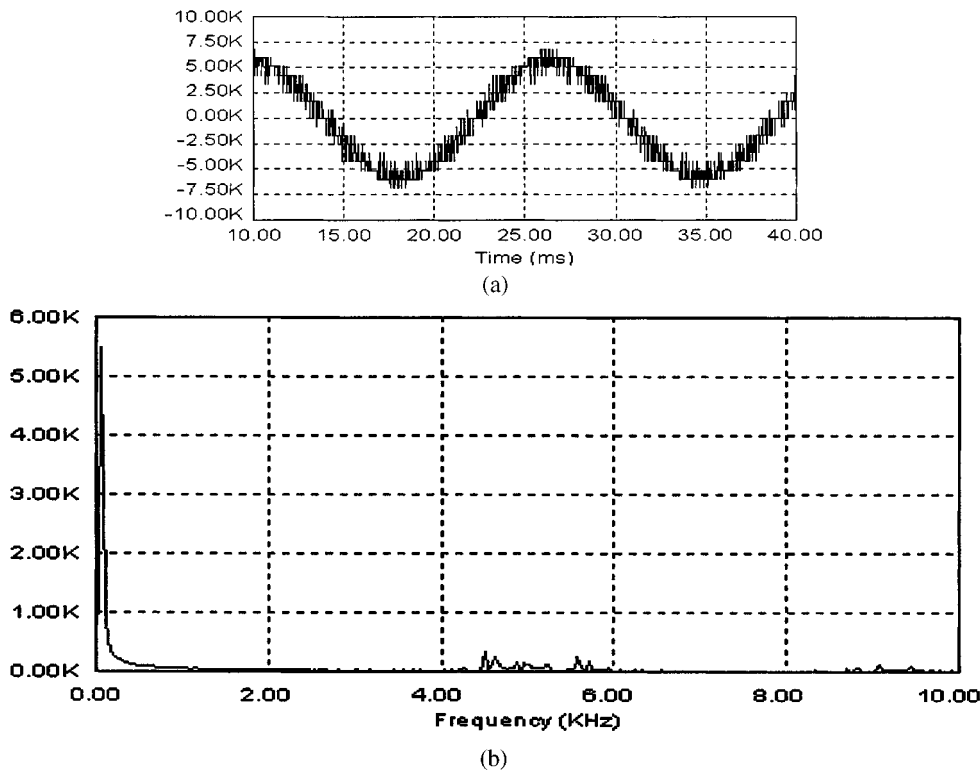


Fig. 7. (a) Example voltage (4160 V, rms) across motor terminals for CML MV-ASD topology with the proposed PWM strategy. (b) The fft of the voltage in Fig. 7(a).

Since each single phase inverter cell has  $0, \pm V_d$  switching states, the worst case value  $V_{AN}$  can assume [see (1)] is

$$V_{AN} = \pm 4V_d. \quad (5)$$

Similarly

$$V_{BN} = V_{CN} = \pm 4V_d. \quad (6)$$

From (4)–(6), the maximum value  $V_{CM}$  can assume is

$$V_{CM, \max} = \pm 4V_d \quad (7)$$

(7) gives the worst case value for common mode voltage or neutral shift in CML-MV-ASD system.

The common mode voltage  $V_{CM}$  [see (4)] generated by cascaded single phase inverter cells due to PWM switching is distributed between the motor winding capacitance to ground and the respective transformer secondary winding capacitances to ground. Since the motor winding capacitance is much larger (150 times) than the transformer secondary winding capacitances to ground, much of the common mode voltage stress is transferred to the transformer. The neutral shift of each transformer secondary winding is also widely different. From the equivalent circuit in Fig. 2, it is easy to infer that the neutral shift is maximum for the transformer secondary winding supplying power to the inverter cell which is closest to the motor. That is, voltage across  $C_{41} \gg$  voltage across  $C_{11}$  (Fig. 2). The exact nature of the transformer secondary windings with respect to ground or neutral shift can be determined via simulations and is discussed in the next section.

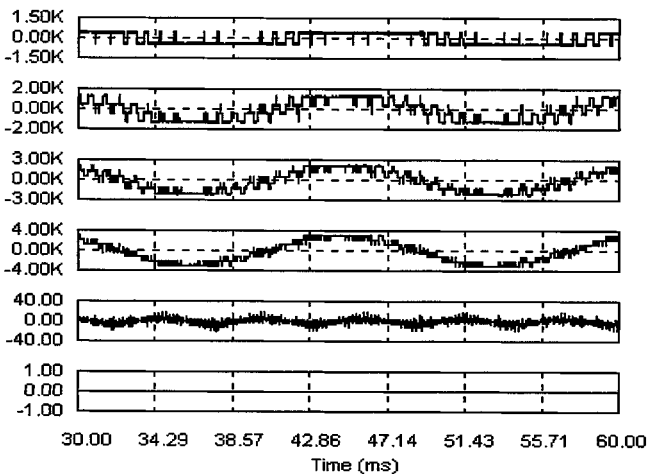


Fig. 8. Voltage potential between neutral points to ground of the phase-a transformers secondaries in the CML inverter topology with the proposed PWM method (see Fig. 2). From top to bottom: voltages  $V_{n_{11},g}$ ,  $V_{n_{21},g}$ ,  $V_{n_{31},g}$ ,  $V_m$ , and  $V_{CM}$ .

### C. Simulation Results

The equivalent circuit of the CML MV-ASD topology (Fig. 2) is simulated to evaluate the common mode voltage or neutral shift on various components. The following data is assumed:

- Inverter dc-link voltage  $V_d = 850$  V;
- Switching frequency  $f_s = 1260$  Hz;
- Number of single-phase inverter cells in each phase = 4;
- $V_{LL, OUTPUT} = 4160$  V (rms);
- Transformer and motor capacitances to ground = see Tables I and II;

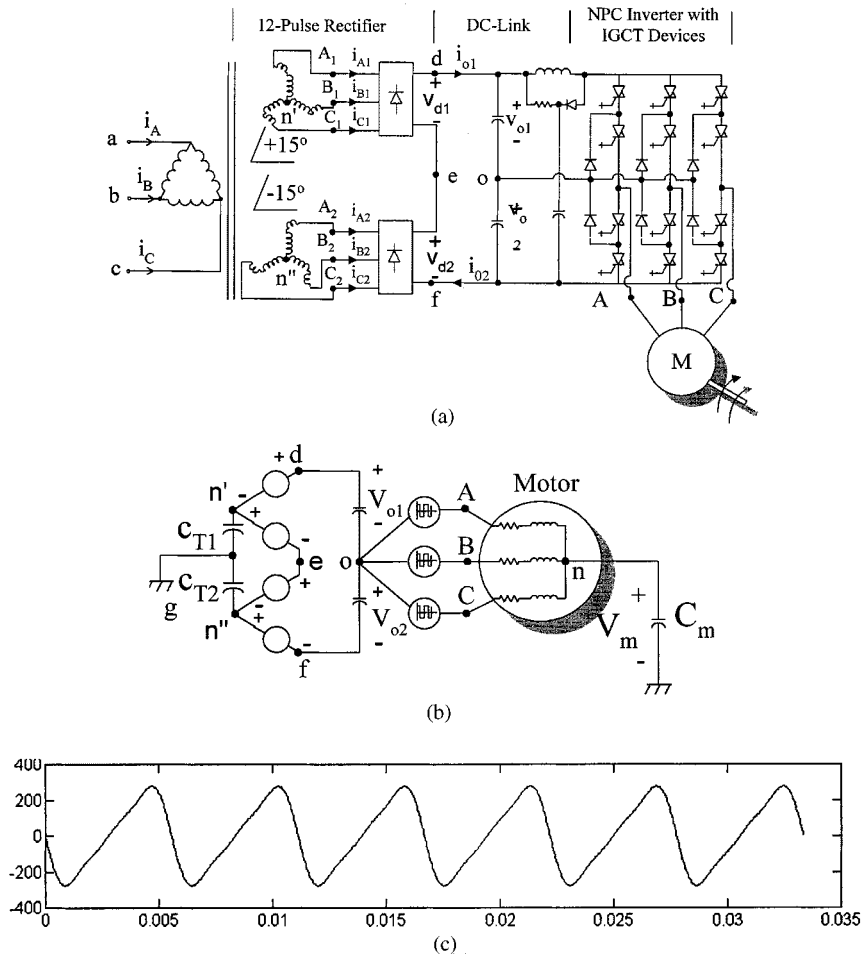


Fig. 9. (a) Three-level NPC Inverter topology for MV-ASD. (b) Common mode equivalent circuit for NPC, MV-ASD (c) Calculated voltage between dc-link midpoint "o" to ground [Eqn. (21)].

PWM strategy = SPWM-unipolar [17], with 45° phase shift between inverter stages.

Fig. 3 shows the line to line voltage across the motor terminals. Fig. 4 shows the simulated waveforms for the voltages  $V_{n_{11},g}$ ,  $V_{n_{21},g}$ ,  $V_{n_{31},g}$ ,  $V_{n_{41},g}$ ,  $V_m$  and  $V_{CM}$  [Fig. 2, Eqn. (4)], respectively. As predicted in the previous section, the transformer secondary powering the inverter cell closest to the motor is more stressed than the transformer secondary power the inverter cell farthest from the motor in the same phase (i.e.  $V_{n_{41},g} \gg V_{n_{11},g}$ ). Another observation is  $V_{CM}$  [computed from Eqn. (4)] is nonzero and is shown to be  $\pm 1800$  V (peak) and has PWM signature. Also, the neutral shift of the motor ( $V_m$ ) is  $\pm 40$  V.

The simulation results demonstrate that transformer secondary windings are subjected to higher common mode voltages than the motor. This is primarily due to the larger value of motor winding capacitance to ground than the transformer (150 times).

#### D. Proposed PWM Strategy to Reduce Common Mode Voltage Stress on the Motor

From the results obtained in previous section (Fig. 4)  $V_{CM}$  was shown to be  $\pm 1800$  V and has PWM signature. It is well known that high  $V_{CM}$  contributes to motor bearing currents and

leakage currents to ground [14]. While bearing currents can degrade bearing life, leakage current can disturb the plant zero-sequence protection [15].

In this section, an advanced strategy is proposed to eliminate  $V_{CM}$  generation. Fig. 5 shows one group of 1-phase inverter cells. For common-mode voltage generated by inverter cells to be zero, it is required that at each instant (Fig. 5)

$$V_{a'_1, a_1} + V_{b'_1, b_1} + V_{c'_1, c_1} = 0. \quad (8)$$

Fig. 6 shows the proposed PWM strategy. Fig. 6(a), (c), and (e) show the intersection of 120° phase-shifted triangle carriers with 120° phase-shifted modulating (sinusoidal plus third harmonic) signals. The gating signals obtained from the intersection are then applied to each inverter cell in Fig. 5 resulting in  $V_{a_1, a'_1}$ ,  $V_{b_1, b'_1}$ ,  $V_{c_1, c'_1}$  [Fig. 6(g)–(i)]. Fig. 6(j) shows the addition of  $V_{a_1, a'_1} + V_{b_1, b'_1} + V_{c_1, c'_1}$  to be zero. The proposed strategy is then adapted to the 4-cascaded inverter stages.

Fig. 7 shows the resultant line to line voltage across the motor terminals with the proposed strategy. Fig. 8 shows the resultant common-mode voltage stresses in the system (obtained from simulation) with the proposed PWM strategy. Comparing Fig. 4 to Fig. 8, the  $V_{CM}$  is zero. It is clear from the simulation results that the proposed PWM strategy results in substantial common-mode voltage reduction.

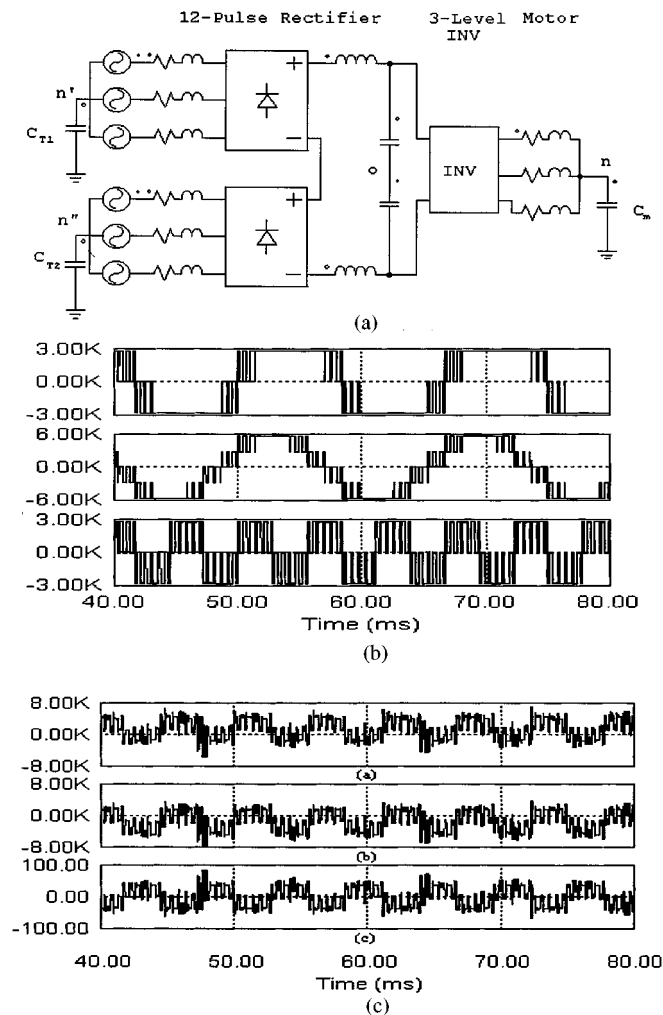


Fig. 10. (a) Simulation circuit diagram for common mode analysis. (b) Top: voltage between inverter terminal "A" and dc-link mid point "o" of the NPC ASD system [see Fig. 9(b)]. Middle: line to line voltage between inverter terminals "A" and "B." Bottom: The resulting common mode voltage  $V_{CM} = V_{Ao} + V_{Bo} + V_{Co}$ . (c) Voltages between transformer secondary neutral points to ground and motor terminals to ground. From top to bottom:  $V_{n',g}$ ,  $V_{n'',g}$ , and  $V_{n,g}$ .

Comparing Fig. 3(b) to Fig. 7(b), it is observed that the proposed PWM strategy increases the harmonic content of the motor terminal voltage.

### III. COMMON MODE VOLTAGE IN 3-LEVEL NPC MV-ASD SYSTEMS

In this section, analysis of common-mode voltage in three-level NPC based medium voltage ASD systems is discussed.

Fig. 9(a) shows the general topology of a commercially available 3-level NPC Inverter for MV-ASD's [10], [13]. The NPC inverter employs IGCT devices [10], [13] and 12-pulse rectifier type utility interface to supply the dc-link. For a 4160 V output, the dc-link voltage is 6000 V with 3000 V across each dc-link capacitor. Each IGCT switch is rated for 6000 V and the overall inverter is suitably PWM controlled to generate a 3-level output. The switching frequency of IGCT inverter is set between 200 Hz and 1 kHz.

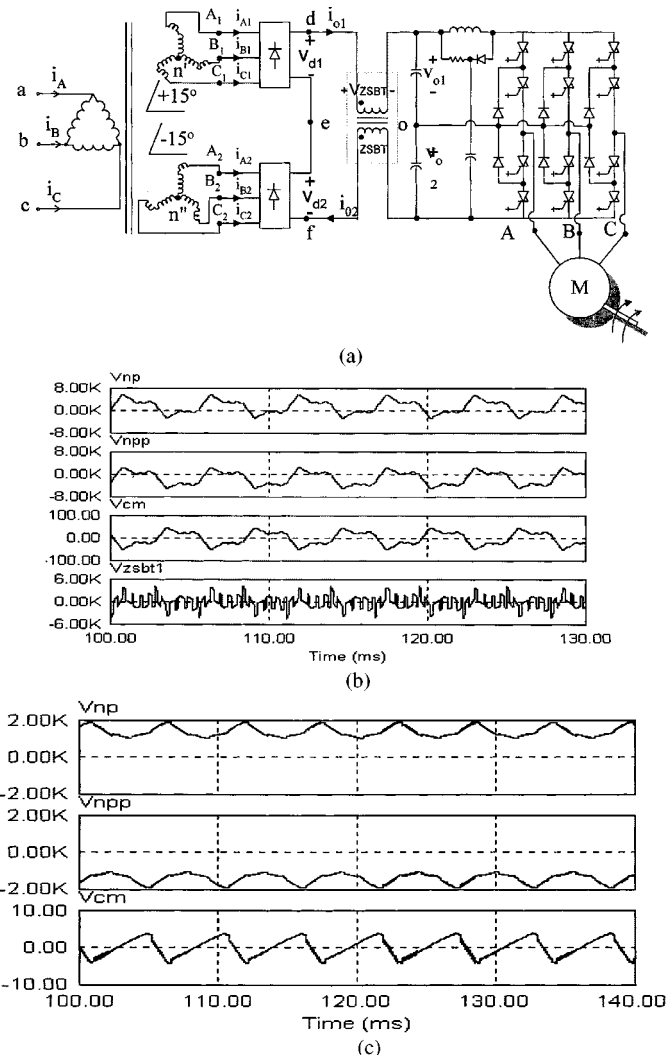


Fig. 11. (a) The proposed ZSBT connection to reduce common-mode voltage excursion at motor terminals and transformer secondary windings. (b) Voltages between secondary transformers neutral points to ground, and motor terminals to ground, and voltage across the ZSBT. From top to bottom:  $V_{n',g}$ ,  $V_{n'',g}$ ,  $V_{n,g}$ , and  $V_{ZSBT1}$ . (c) Voltages between secondary transformer/motor neutral points to ground when common mode cancellation scheme is applied to the NPC inverter [ $V_{on} = 0$  in Fig. 9(b)]. From top to bottom:  $V_{n',g}$ ,  $V_{n'',g}$ , and  $V_{n,g}$ .

#### A. Common Mode Equivalent Circuit of NPC-MV ASD

Fig. 9(b) shows the equivalent circuit derived from Fig. 9(a) of the 3-level MV-ASD system for the purpose of common mode voltage analysis. The common mode voltage at the motor terminals is

$$V_{CM} = \frac{V_{Ag} + V_{Bg} + V_{Cg}}{3} \quad (9)$$

where

$$V_{Ag} = V_{Ao} + V_{og} \quad (10)$$

$$V_{Bg} = V_{Bo} + V_{og} \quad (11)$$

$$V_{Cg} = V_{Co} + V_{og} \quad (12)$$

therefore

$$V_{CM} = \frac{V_{Ao} + V_{Bo} + V_{Co}}{3} + V_{og}. \quad (13)$$

To derive  $V_{og}$ , the following equations can be written for

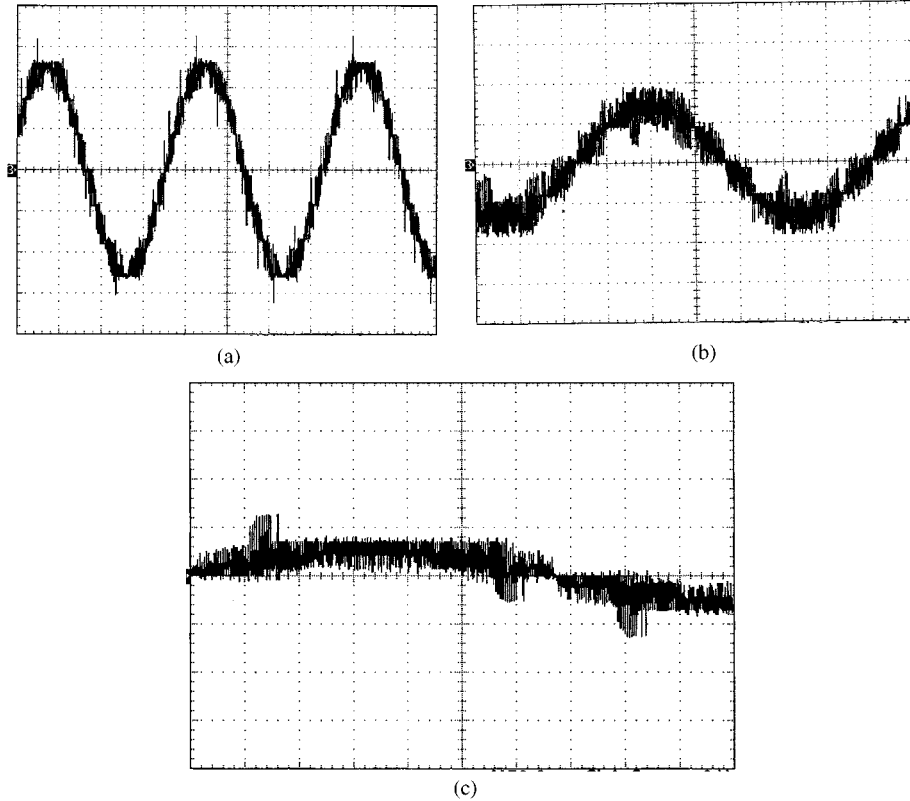


Fig. 12. (a) Motor line to line voltage at 90% speed (scale: 2 kV/div, 5 ms/div). (b) Motor line to line voltage at 50% speed (scale: 2 kV/div, 5 ms/div). (c) Motor line to line voltage at 25% speed (scale: 2k V/div, 5 ms/div).

Fig. 9(b)

$$V_{de} = V_{dn'} - V_{en'} \quad (14)$$

$$V_{ef} = V_{en''} - V_{fn''} \quad (15)$$

next

$$V_{df} = V_{de} + V_{ef} \quad (16)$$

$$V_{do} = \frac{V_{df}}{2} = \frac{V_{de} + V_{ef}}{2}. \quad (17)$$

Substituting (14) and (15) into (17), we have

$$V_{do} = \frac{V_{dn'} - V_{en'} + V_{en''} - V_{fn''}}{2} \quad (18)$$

also

$$V_{n'g} = \frac{V_{n'e} + V_{en''}}{2} \quad (19)$$

and

$$V_{og} = V_{n'g} + V_{dn'} - V_{do}. \quad (20)$$

Substituting (18) and (19) into (20) we obtain

$$V_{og} = \frac{V_{dn'} + V_{fn''}}{2}. \quad (21)$$

Fig. 9(c) shows the calculated voltage waveforms of  $V_{og}$  in (21).

### B. Simulation of the NPC, MV-ASD System

The equivalent circuit shown in Fig. 9(b) is used for simulation purposes and the schematic diagram is shown in Fig. 10(a). The coupling capacitances between transformer secondary neutrals and motor neutral to ground are represented by  $C_{T1}$ ,  $C_{T2}$ ,

and  $C_m$ , respectively. And their values are assumed to be  $C_{T1} = C_{T2} = 400$  pF, and  $C_m = 65$  nF. Fig. 10(b) shows the resulting common mode voltages due to the inverter switching from simulations.

Fig. 10(c) shows the common-mode voltages distribution in a three-level NPC system. Notice that the voltages between transformers' secondary neutrals to ground are much higher than the voltage between motor's neutral to ground. This is true since the equivalent coupling capacitance's to ground of the transformer ( $C_{T1}$ ,  $C_{T2}$ ) are normally much smaller than that of the equivalent coupling capacitance of the motor neutral to ground  $C_m$ . The common mode voltage that appears between the motor neutral to ground may cause induced shaft voltages, bearing currents, and circulating bearing currents [16].

### C. Use of ZSBT to Reduce Common Mode $dv/dt$ for NPC, MV-ASD

In this section, simulation results on the use of a zero sequence blocking transformer (ZSBT) to reduce the common-mode stress is discussed. The connection of the ZSBT is shown in Fig. 11(a). A ZSBT is basically a transformer with two windings wound on a common core. The use of ZSBT reduces the common mode voltage between motor terminals to ground and from the transformer secondary terminals to ground. Fig. 11(b) shows the voltages of transformer secondary terminals to ground, motor terminals to ground and across the ZSBT windings. With the ZSBT in place, the common-mode voltages across the coupling capacitances exhibit low  $dv/dt$ 's as expected.

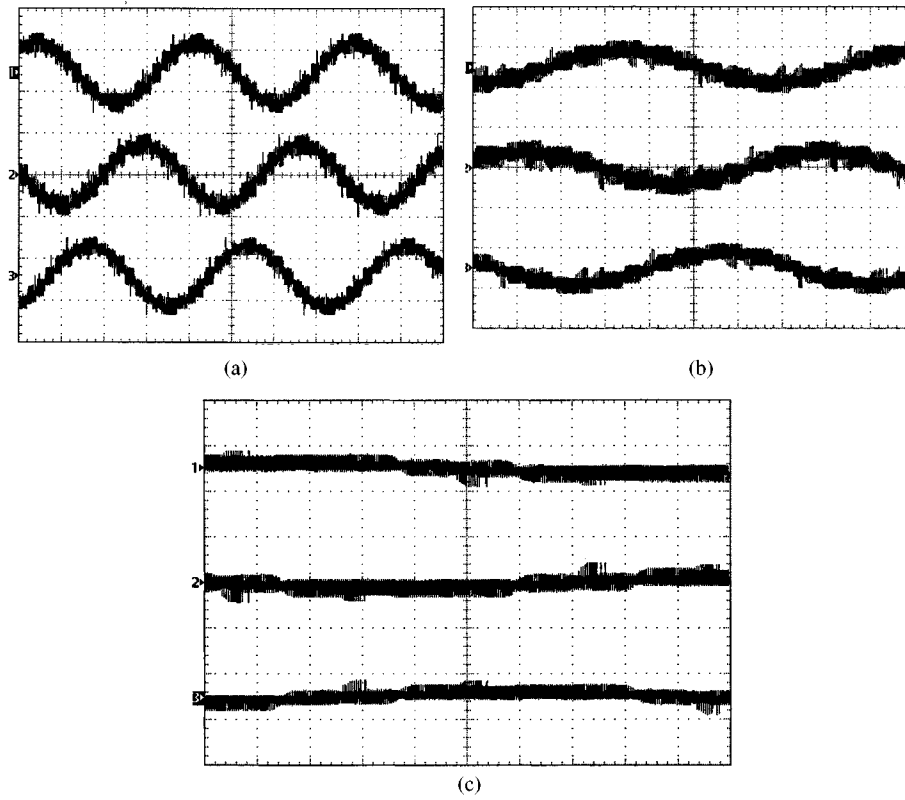


Fig. 13. (a) Motor terminal voltages to ground  $V_{ag}$ ,  $V_{bg}$ , and  $V_{cg}$  at 90% speed (scale: 4 kV/div, 5 ms/div). (b) Motor terminal voltages to ground  $V_{ag}$ ,  $V_{bg}$ , and  $V_{cg}$  at 50% speed (scale: 4 kV/div, 5 ms/div). (c) Motor terminal voltages to ground  $V_{ag}$ ,  $V_{bg}$ , and  $V_{cg}$  at 25% speed (scale: 4 kV/div, 5 ms/div).

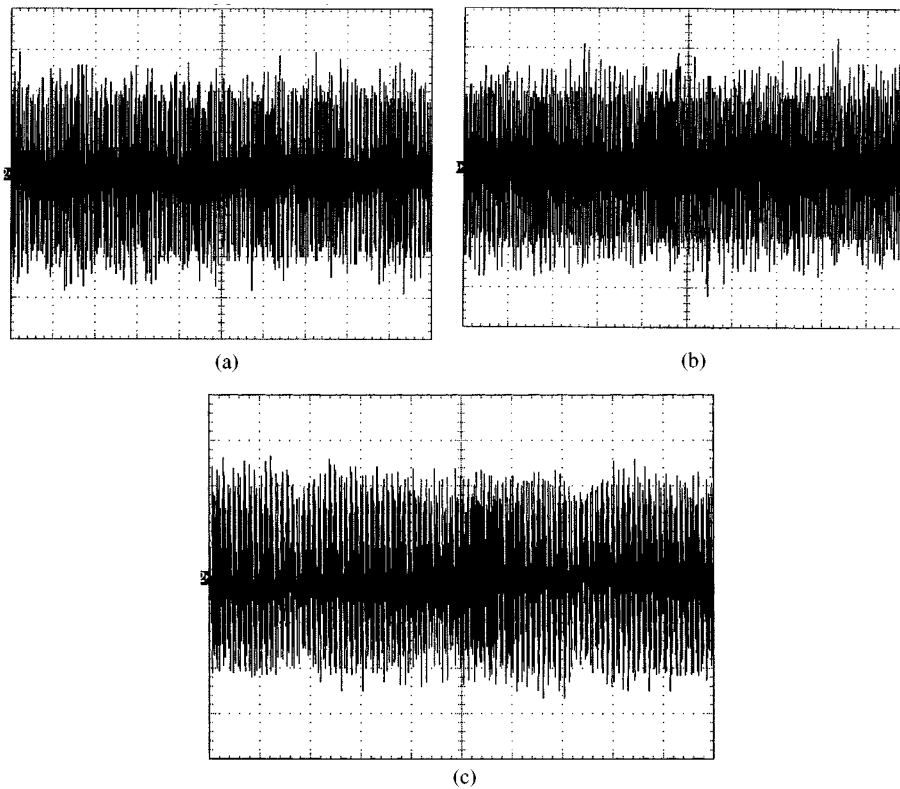
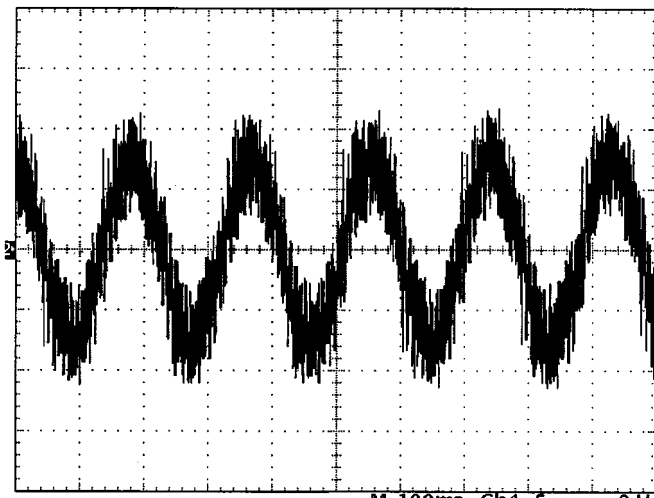
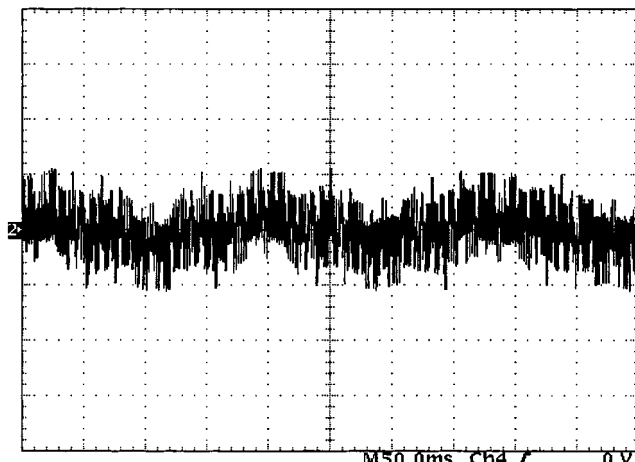


Fig. 14. (a) Common mode voltage at motor terminals to ground at 90% speed (scale: 1 kV/div, 2 ms/div). (b) Common mode voltage at motor terminals to ground at 50% speed (scale: 1 kV/div, 2 ms/div). (c) Common mode voltage at motor terminals to ground at 25% speed (scale: 1 kV/div, 2 ms/div).



(a)



(b)

Fig. 15. (a) Voltage between ground and transformer secondary terminals in phase-A closest to motor at 90% speed,  $V_{n_{41},g}$  (scale: 5 kV/div, 10 ms/div). (b) Voltage between ground and terminals of transformer secondary in phase-A farthest to motor at 90% speed,  $V_{n_{11},g}$  (scale: 5 kV/div, 10 ms/div).

A PWM strategy to eliminate the common mode voltage can also be applied to the NPC inverter [12] to reduce various voltage stresses in the system. Fig. 11(c) shows the voltages of transformer secondary terminals to ground and motor terminals to ground when a common-mode cancellation technique [12] is applied to the NPC inverter. It is clear that, this method results in the most reductions of common mode  $dv/dt$ 's. However, this approach causes 13% reduction of fundamental voltage across the motor terminals.

#### IV. EXPERIMENTAL RESULTS

In this section, experimental results from a 4160, 800 hp, 4-pole medium voltage induction motor, CML-MVD-ASD system are presented. Each inverter cell is operated with  $V_d = 850$  V, switching frequency  $f_s = 1260$  Hz. Various system voltages were measured under no load. The medium voltage motor was isolated from the ground to measure the leakage current to ground accurately. Since the motor did not have insulated bearings, induced shaft voltage to ground could not be measured accurately.

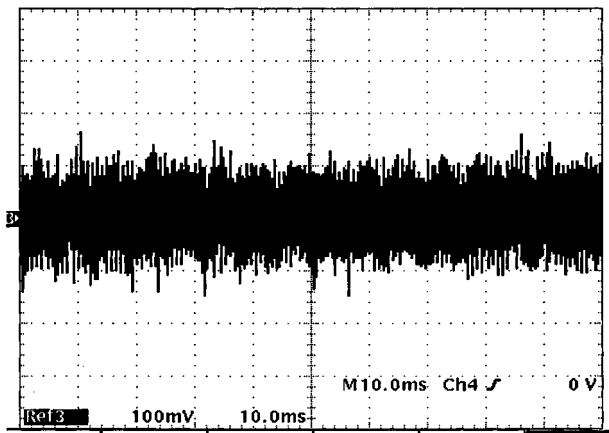


Fig. 16. Motor leakage current to ground at 90% speed (scale: 1 A/div, 10 ms/div).

Fig. 12(a)–(c) show the motor line to line voltage at 90%, 50%, and 25% speeds. Fig. 13(a)–(c) show the measured motor terminal voltages to ground at 90%, 50%, and 25% speeds. Fig. 14(a)–(c) show the resultant common-mode voltage across the motor terminals. These waveforms were obtained by the addition of three motor terminal voltages to ground (in Fig. 13) on a digitizing oscilloscope. It is interesting to note that the measured common mode voltage across the motor terminals is nearly constant at each speed and consists of PWM pulses from various inverter switching states. Fig. 15 show the neutral shift voltages of two secondary windings of the input transformer (these voltages represent the summation of three secondary winding voltages measured with respect to ground). Fig. 15(a) shows the neutral shift voltage of transformer secondary winding powering the inverter cell #4, which is closest to the motor (Fig. 1). Fig. 15(b) shows the neutral shift voltage of transformer secondary winding powering inverter cell #1, which is farthest from the motor. It is clear from Fig. 15(a), (b) that the two secondary windings are unevenly stressed. Fig. 16 shows the measured leakage current to ground at 90% speed.

#### V. CONCLUSIONS

In this paper, analysis of common mode voltage or neutral shift in voltage source type MV-ASD system has been presented. Both CML-MV-ASD and NPC-MV-ASD have been analyzed. Simulation and experimental results have been shown to verify analytical predictions. New PWM strategy to reduce the common mode voltage generated by inverter switching have been suggested. The advantage of this approach will be to minimize bearing currents and leakage currents to ground. It has been shown that the input transformer secondary windings in CML-MV-ASD are subjected to uneven stress and this data is useful during the design stage. Finally, experimental results on a 4160 V, 800 hp, CML-MV-ASD have been presented.

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