

# A New Approach to Mitigate Nuisance Tripping of PWM ASDs due to Utility Capacitor Switching Transients (CSTs)

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**Abstract**—Utility capacitor-switching transients (CSTs) are responsible for numerous nuisance tripping of PWM adjustable speed drives (ASDs) and result in costly down times. During a CST event, the dc link voltage of the ASD can momentarily rise to greater than 1.3 p.u. resulting in nuisance tripping. In this paper, a new approach to mitigate nuisance tripping of PWM ASDs is discussed. In this approach, the soft-charge resistor available in most ASDs, is momentarily introduced in the series path of the power flow to effectively damping the CST. Further, damping effect is electronically adjusted. The proposed approach demonstrates a method that can be incorporated within an ASD to electronically damp the oscillatory transient generated during a CST event. The advantages of the proposed approach are

- i) electronic damping for CST event is achieved by low cost modifications to ASD hardware;
- ii) it adapts to several utility resonance conditions.

The required additional hardware for ASDs to be immune to CSTs, can be viewed as an add-on option. This paper discusses the analysis, simulation and experimental performance on a 480 V, 16 kVA commercial ASD equipment.

**Index Terms**—Adjustable speed drives, capacitor switching transients, electronic damping, power quality.

## I. INTRODUCTION

THE application of adjustable speed drives (ASDs) in commercial and industrial facilities is increasing due to their improved efficiency, energy savings and electronic process control. However, modern ASD equipment is more susceptible to utility transients such as: sags [1]–[3], swells, short-term power interruptions, and utility capacitor-switching events [2]–[5]. Voltage sags generally cause under-voltage trip in an ASD [2]. A short-term power interruption for a few cycles, results in rapid decrease in ASD dc link voltage and requires an appropriate energy storage for ride-through [3]. On the other hand, a voltage swell or a capacitor switching transient (CST), results in a momentary increase in dc link voltage ( $>1.3$  p.u.) and most often results in an overvoltage trip [5], [8]–[10], [12], [15]. The utility CST is the most common cause of transient overvoltages, second only to lightning in frequency of occurrence in most systems [6], [13]. In ASD equipment, the dc link capacitor  $C_d$  along with dc link inductance  $L_d$  along with

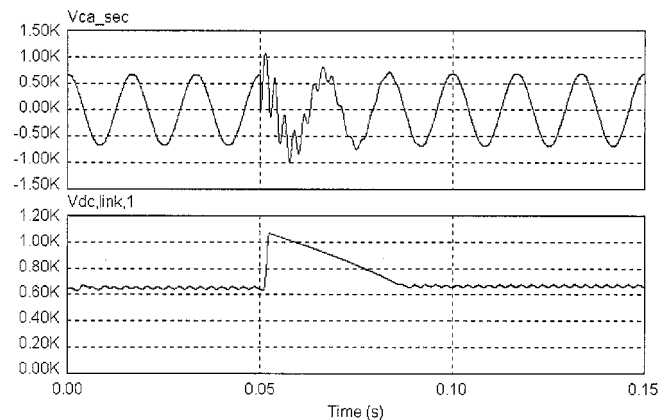


Fig. 1. Typical capacitor switching transient and the overvoltage occurrence in an ASD dc link.

utility line inductance  $L_s$  form an  $LC$  resonant circuit. During a CST event, the  $LC$  resonant circuit is excited and a current surge is produced, resulting in rise of dc link voltage ( $>1.3$  p.u.). In order to protect the IGBTs and diodes, overvoltage trip generally occurs, resulting in a nuisance tripping of the ASD. Fig. 1 illustrates a typical CST event and the momentary rise in the ASD dc link voltage. Fig. 1 shows a line-to-line voltage,  $V_{ca,sec}$  in the secondary side of a distribution substation, as shown in Fig. 2. In Fig. 1, it is also shown the term  $V_{dc,link,1}$ , which represents the ASD dc link voltage on ASD1 in a typical power system (Fig. 2).

Power quality concerns due to CST events have been widely recognized in the literature [1], [6]–[10]. Common mitigation methods to prevent nuisance tripping of ASDs so far suggested include [4]–[8], [15].

- i) Installing of 3–5% of additional line reactance in front of the ASD. This approach alters the  $LC$  resonance and reduces the overvoltage. However, additional inductance increases the susceptibility of ASDs tripping for common voltage sags [2].
- ii) Suggested mitigation methods which can be implemented by the utility include [6]–[8], [11], [12], [14]: employ preinsertion resistors/inductors during capacitor switching [6], [8]; employ high-speed/static circuit breakers with zero-voltage closing control [6]–[8], [14]. These solutions have to be implemented by electric utility and are expensive.

In response to these concerns, this paper explores a new approach to mitigate nuisance tripping of PWM ASDs due to

Manuscript received August 4, 2000; revised April 18, 2002. Recommended by Associate Editor L. Moran.

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Publisher Item Identifier 10.1109/TPEL.2002.802198.

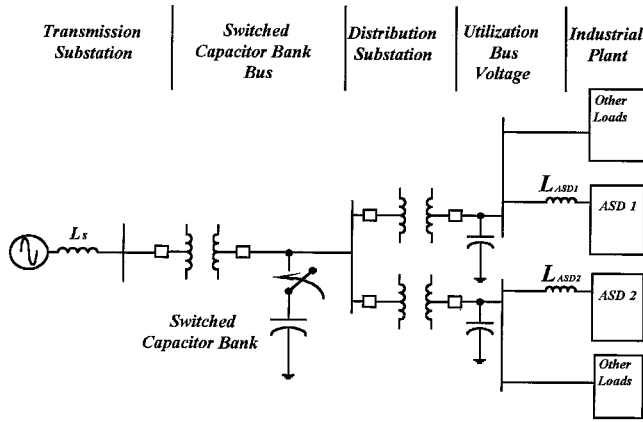


Fig. 2. Example of a one-line diagram of a typical power system.

utility capacitor switching transient (CST) events. Modifications to ASD hardware are suggested to electronically damp the CST event, thus avoiding overvoltage in the dc link and preventing nuisance tripping of ASDs. In this approach the soft-charge resistor available in most ASDs, is momentarily introduced in the series path of the power flow to effectively damping the CST. The soft-charge resistor can be introduced along with a dc link inductance (reactor),  $L_d$ , available in most ASD equipment. Further, damping effect is electronically adjustable.

## II. ANALYSIS OF CAPACITOR SWITCHING TRANSIENT EVENTS

Utilities often use capacitor banks to maintain the distribution voltage level under varying load demands. The utility CST event is a relatively common power-system phenomena. Fig. 2 illustrates a typical utility CST event in a power distribution system.

### A. Analysis

In order to evaluate the effect of utility CST on ASDs, a simplified representation and an equivalent circuit of the power system is shown in Fig. 3.

Fig. 3(a) illustrates the simplified representation for a CST event in a typical power system. The analysis can be simplified by modeling the power system as an  $LC$  circuit [Fig. 3(b)] for the transient response [16].

From Fig. 3(b) the following differential equation can be written:

$$L_{\text{eff}} \frac{d}{dt} i(t) + \frac{1}{C_{\text{eff}}} \int i(t) dt = v(t) \quad (1)$$

where  $L_{\text{eff}}$  is the effective line inductance and  $C_{\text{eff}}$  is the effective capacitance being switched. Defining, the characteristic impedance  $Z_0$

$$Z_0 = \sqrt{\frac{L_{\text{eff}}}{C_{\text{eff}}}} \quad (2)$$

and the resonant frequency

$$\omega_n = \frac{1}{\sqrt{L_{\text{eff}} C_{\text{eff}}}}, \quad n = \frac{\omega_n}{\omega} \quad (3)$$

Where  $n$  is the per-unit natural frequency and  $\omega$  is the fundamental power system frequency.

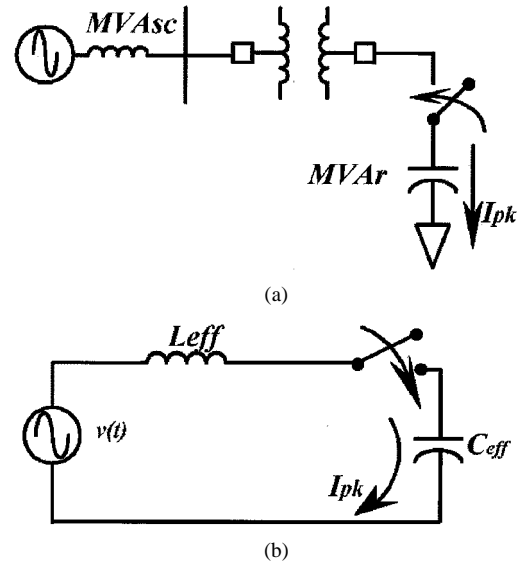


Fig. 3. Equivalent circuit of the power system for the capacitor switching transient event: (a) simplified representation and (b) equivalent circuit.

Also, defining the peak current

$$I_{\text{pk}} = \frac{V_{\text{pk}}}{Z_0} \quad (4)$$

where  $V_{\text{pk}}$  is the peak value of the fundamental frequency voltage.

The peak value of the capacitor voltage  $V_{\text{pk}}$  can be expressed as

$$V_{\text{pk}} = I_{\text{pk}} Z_0 \left( \frac{n^2}{n^2 - 1} \right). \quad (5)$$

The worst case of the voltage peak may occur on re-striking the capacitor bank with a trapped charge of 1 p.u. In this case, if the re-strike occurs when the source voltage reaches its peak, the voltage across the contacts of the switch will be two times the source peak system voltage as defined by

$$V_{\text{pk,crit}} = V_{\text{pk}} - (-V_{C_{\text{eff}}}) = 2V_{\text{pk}}. \quad (6)$$

The instantaneous current in this case can be expressed as

$$I_{\text{pk}} = \frac{2V_{\text{pk}}}{Z_0}. \quad (7)$$

### B. Effect of Utility CST on ASDs

In this section the effect of a utility CST event on an ASD is examined. Fig. 4(a) shows the topology of a typical ASD. Fig. 4(b) shows the equivalent circuit for analysis. In Fig. 4(b),  $V_s$  and its symbol represent the line-to-line voltage applied to the ASD system, which is short-circuited at the event of a CST event and can reach a critical peak value given by (6).

From the equivalent circuit [Fig. 4(b)] we have

$$L_{\text{eff}} \frac{d}{dt} i_d(t) = -v_{\text{dc}}(t) - V_{\text{dc}}(0^+) + v_s(t) \quad (8)$$

$$v_{\text{dc}}(t) + V_{\text{dc}}(0^+) = R_o i_{d,\text{av}}(t) \quad (9)$$

$$C_d \frac{d}{dt} v_{\text{dc}}(t) = i_d(t) - i_{d,\text{av}}(t). \quad (10)$$

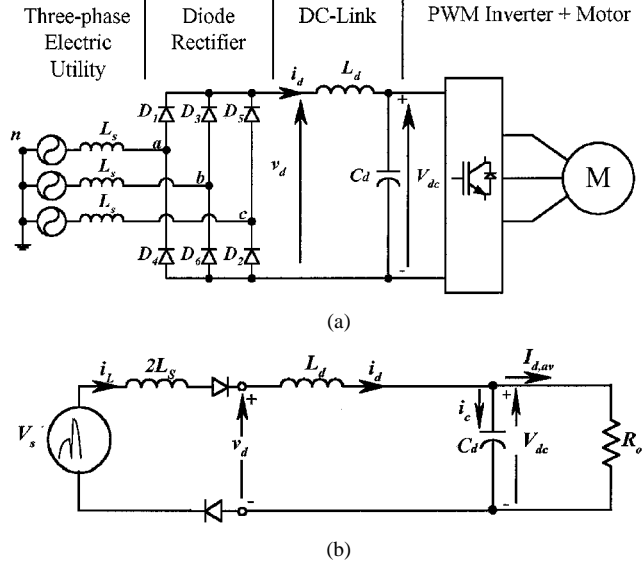


Fig. 4. Adjustable speed drive: (a) typical ASD topology and (b) equivalent circuit of an ASD under a CST event.

Where  $L_{\text{eff}} = 2L_s + L_d$  represents the effective ASD input inductance. The utility input voltage ( $V_s$ ) represents the source voltage with a magnitude equal to two times the maximum line-to-line voltage (for a worst case CST). Also, the steady-state  $V_{\text{dc}}$  is [17]

$$V_{\text{dc}} = 1.35V_{\text{LL}}. \quad (11)$$

From (8), (9), and (10), a time-domain equation for the ASD dc link voltage is derived as

$$\frac{v_{\text{dc}}(t)}{(2\sqrt{2})V_{\text{LL}}} = \left[ 1 - \frac{e^{-\zeta\omega_n t}}{\sqrt{1-\zeta^2}} \sin(\omega_n \sqrt{1-\zeta^2} t + \theta) + \frac{1.35}{(2\sqrt{2})} e^{-\zeta\omega_n t} \cos(\omega_n \sqrt{1-\zeta^2} t) \right] \quad (12)$$

where the resonant frequency is defined as

$$\omega_n = \sqrt{\frac{1}{L_{\text{eff}}C_d}}. \quad (13)$$

The damping ratio is expressed as

$$\zeta = \frac{1}{2R_o} \sqrt{\frac{L_{\text{eff}}}{C_d}} \quad (14)$$

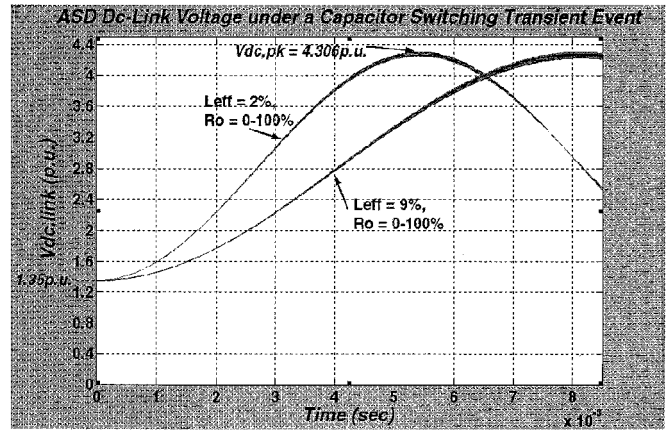
$$\theta = \tan^{-1} \left( \frac{\sqrt{1-\zeta^2}}{\zeta} \right). \quad (15)$$

Evaluating (12), the peak time  $t_{\text{pk}}$  can be expressed as

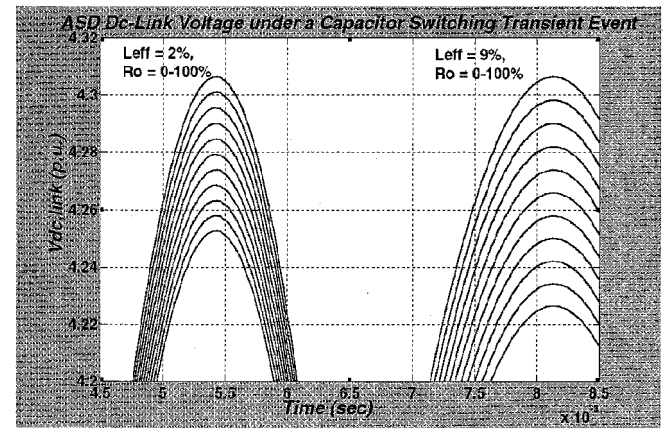
$$t_{\text{pk}} = \frac{\pi}{\omega_n \sqrt{1-\zeta^2}}. \quad (16)$$

The ASD dc link voltage peak can be computed from (12) at the time defined by (16), as expressed in per-unit quantity by

$$V_{\text{dc,pk}} = 2\sqrt{2} + \sqrt{2} \left[ \frac{2\pi - 3}{\pi} \right] \frac{e^{-\frac{\zeta}{\sqrt{1-\zeta^2}}\pi}}{\sqrt{1-\zeta^2}} \sin(\theta). \quad (17)$$



(a)



(b)

Fig. 5. ASD dc link voltage transient response under a CST event with  $L_{\text{eff}} = 2L_s + L_d$ .

### C. Effect of Line Inductance $L_s$ and ASD Load ( $R_o$ ) on $V_{\text{dc,pk}}$

In this section, the effect of line input inductance  $L_{\text{eff}}$  and ASD load,  $R_o$  [Fig. 4(b)] on  $V_{\text{dc,pk}}$  is explored. The following per-unit quantities are defined:

utility line-to-line voltage  $V_{\text{LL}} = 1$  p.u.

input power ASD  $V_A = 1$  p.u.

dc link voltage  $V_{\text{dc}} = 1.35$  p.u.

Fig. 5 shows the variation of  $v_{\text{dc}}(t)$  as a function of time and for different  $L_s$  and  $R_o$  values, in per unit. Fig. 5(b) shows the expanded version of Fig. 5(a) around the peak of  $v_{\text{dc}}(t)$ . It is clear from Fig. 5(a) and (b) that for lower values of  $L_{\text{eff}}$ , the rate of rise of  $v_{\text{dc}}(t)$  from nominal (1.35 p.u.) to  $V_{\text{dc,pk}}$  (4.31 p.u.) is shorter. Also, the ASD load ( $R_o$ ) has negligible effect on the  $V_{\text{dc,pk}}$  [Fig. 5(a)].

## III. PROPOSED APPROACH TO MITIGATE NUISANCE TRIPPING OF ASDs UNDER UTILITY CST EVENTS

In this section, a new method to mitigate nuisance tripping of PWM ASDs due to utility capacitor switching events is discussed.

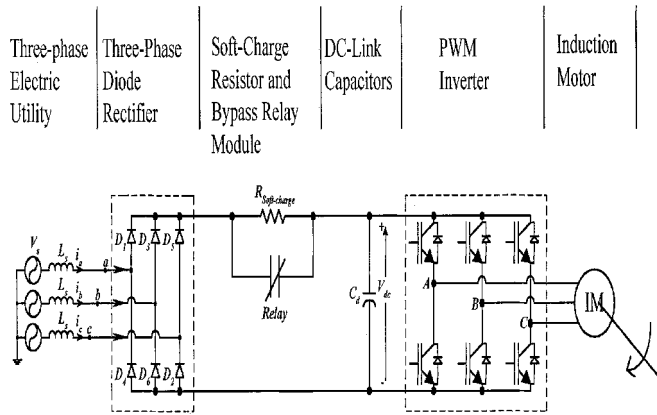


Fig. 6. Conventional topology for a PWM ASD.

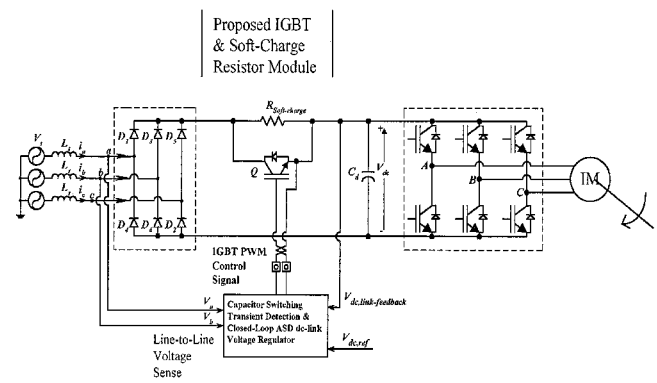


Fig. 7. Proposed approach to mitigate nuisance tripping of PWM ASDs due to CSTs events.

Fig. 6 shows a typical ASD topology, which consists of a three-phase diode rectifier, dc link, and a PWM inverter. A soft-charge resistor ( $R_{\text{soft-charge}}$ ) and a bypass relay module are typically employed in the dc link power flow path of the ASD equipment to prevent overcharge of the dc link capacitor during initial startup. The soft-charge resistor is bypassed by a relay contactor in steady-state, after a predetermined delay by the ASD control circuit. Hence, the dc link power flows through the ASD relay module without any dc voltage drop in the main power flow path.

Fig. 7 shows the proposed approach to mitigate nuisance tripping of PWM ASDs due to CSTs events. In this approach, the relay used to bypass the soft-charge resistor,  $R_{\text{soft-charge}}$  is replaced by an IGBT. Under normal conditions, the IGBT is enabled and  $R_{\text{soft-charge}}$  is effectively short-circuited. However, during a CST event, the IGBT is essentially de-activated and  $R_{\text{soft-charge}}$  is introduced in series with the dc link capacitor  $C_d$  such that  $V_{dc}$  transient is effectively damped. Further, the value of effective damping resistance  $R_{\text{soft-charge}}$  can be adjusted by suitably modulating the on-off time of the IGBT. This feature facilitates electronic control and suitable damping can be achieved for various types of CST events and varying utility line impedance. Fig. 8 shows the block diagram for the detection and feedback control scheme to mitigate nuisance tripping of PWM ASDs due to CST events.

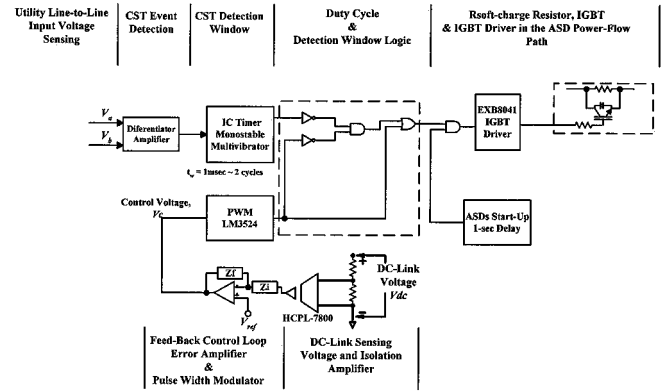
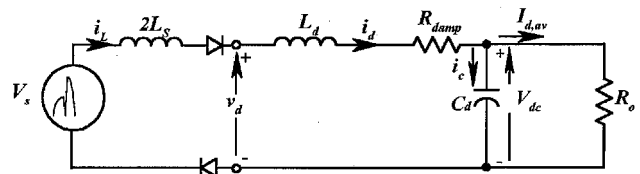


Fig. 8. Detection and feedback control scheme to mitigate nuisance tripping of PWM ASDs due to CST events.

Fig. 9. Equivalent circuit of an ASD under a CST event with damping resistance  $R_{\text{damp}}$ .

In Fig. 8, the detection and control scheme senses the line-to-line voltage, let say  $V_{ab}$ . A differentiator amplifier detects the fast change in the line-to-line voltages due to CST events. The CST event detection enables a monostable multivibrator, which activates a pulse width detection window given by a preset window time value  $t_w$  (1 ms ~ 2 cycles). The pulse width detection window along with the duty cycle of the PWM will activate and de-activate the IGBT accordingly to the logic circuit shown in Fig. 8. A dc link-sensing voltage is also implemented to achieve a feedback control loop through a basic error amplifier scheme. This control scheme will keep the modulation of the IGBT &  $R_{\text{soft-charge}}$  resistor to effectively damp the dc link voltage under a CST event. The effective damping resistance value,  $R_{\text{damp}}$ , applied to mitigate the over-voltage will be given by the modulating function of the control scheme shown in Fig. 8. The damping resistance,  $R_{\text{damp}}$ , will be a direct function of the duty cycle applied to the IGBT and the value of the ASD soft-charge resistance  $R_{\text{soft-charge}}$ .

#### A. Analysis

In this section an in depth analysis is presented to compute the required amount of damping resistance " $R_{\text{damp}}$ " to limit the dc link voltage overshoot. Fig. 9 shows the equivalent circuit when a CST event occurs and  $R_{\text{damp}}$  is introduced in the circuit.

From Fig. 9 we have

$$L_{\text{eff}} \frac{d}{dt} i_d(t) = -R_{\text{damp}} i_d(t) - v_{\text{dc,link}}(t) - V_{\text{dc}}(0^+) + v_s(t) \quad (18)$$

$$v_{\text{dc}}(t) + V_{\text{dc}}(0^+) = R_o i_{d,\text{av}}(t) \quad (19)$$

$$C_d \frac{d}{dt} v_{\text{dc}}(t) = i_d(t) - i_{d,\text{av}}(t). \quad (20)$$

The solution for the  $v_{dc}(t)$  from (18)–(20) is

$$\begin{aligned} \frac{v_{dc}(t)}{(2\sqrt{2})V_{LL}} &= \frac{R_o}{R_{damp} + R_o} \left[ 1 - \frac{1}{\sqrt{1-\zeta^2}} e^{-\zeta\omega_n t} \right. \\ &\quad \times \left. \sin(\omega_n \sqrt{1-\zeta^2} t + \theta) \right] \\ &\quad + \frac{1.35}{(2\sqrt{2})} e^{-\zeta\omega_n t} \cos(\omega_n \sqrt{1-\zeta^2} t) \end{aligned} \quad (21)$$

where

$$\omega_n = \sqrt{\frac{R_{damp} + R_o}{L_{eff} R_o C_d}} \quad (22)$$

$$\zeta = \frac{L_{eff} + R_{damp} R_o C_d}{2\sqrt{(R_{damp} + R_o)(L_{eff} R_o C_d)}} \quad (23)$$

$$\theta = \tan^{-1} \left( \frac{\sqrt{1-\zeta^2}}{\zeta} \right). \quad (24)$$

### B. Damping Resistance

Equation (21) shows the variation of  $v_{dc}(t)$  when  $R_{damp}$  is introduced into the circuit. By evaluating (21) for

$$\begin{aligned} v_{dc}(\infty) &= v_{dc}(t) \\ t &\rightarrow \infty. \end{aligned} \quad (25)$$

And limiting  $V_{dc,pk} = v(\infty)$  to  $V_{dc,trip} = 130\%$ , we have

$$V_{dc,pk} = 1.3 * 1.35 \text{ p.u.} \quad (26)$$

Substituting (26) in (21) and evaluating for  $t = \infty$ , the required value of  $R_{damp}$  can be computed as

$$\begin{aligned} R_{damp} &= \left[ \frac{2\sqrt{2}}{1.35 * V_{dc,trip}} - 1 \right] R_o \text{ p.u.} \\ R_{damp} &= (0.61) R_o \text{ p.u.} \end{aligned} \quad (27)$$

The damping resistance as a function of the duty cycle ( $D$ ) (Fig. 8) and soft-charge resistance can be defined as

$$R_{damp} = (1 - D) R_{soft-charge}. \quad (28)$$

## IV. DESIGN EXAMPLE

In this section, a design example is presented for a 480-V, 60-Hz, 16-kVA commercial ASD equipment. Fig. 7 shows the hardware implementation of the proposed approach. The following quantities are defined.

$$\text{Utility line-to-line voltage} = V_{base} = V_{LL} = 480 \text{ V} = 1 \text{ p.u.}$$

$$\text{Line impedance} = Z_{L,SYS} = 3\% Z_{base}.$$

$$\text{ASD power rating} = S_{ASD} = 16 \text{ kVA} = 1 \text{ p.u.}$$

$$\text{Power factor} = \text{p.f.} = 0.7.$$

$$\text{Power system frequency} = 60 \text{ Hz.}$$

$$\text{Damping ratio [16]} = \lambda = 0.2.$$

$$\text{Integrated ASD } R_{soft-charge} = 20 \Omega.$$

$$\text{Output power, } P_{asd} = \text{pf}(S_{asd}) = 0.7 \text{ p.u.}$$

$$\text{DC Link capacitor, } C_d = 1950 \mu\text{F} = 9.45\% (Z_{base}).$$

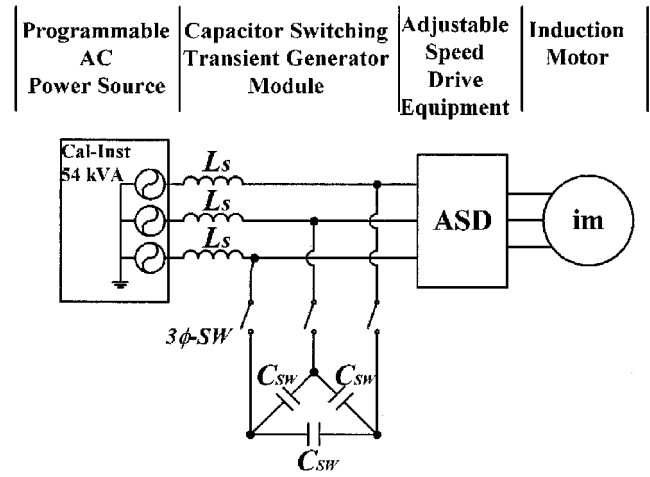


Fig. 10. Experiment setup for initiating a CST event.

TABLE I  
CHARACTERISTIC TRANSIENT COMPONENTS IN A UTILITY CST EVENT AFFECTING AT THE INPUT OF A 480 V, 16 kVA, 60 Hz, ASD EQUIPMENT

$C_{sw}$ ( $\mu\text{F}$ )	$Q_c$ (kVAr)	$Z_o$ ( $\Omega$ )	$f_n$ (Hz)	$V_{pk}$ (V)	$V_{pk,crit}$ (kV)
30	7.82	3.0	593	685	1.37
60	15.64	2.1	420	693	1.39
90	23.45	1.7	342	700	1.40
140	36.48	1.4	275	712	1.42

ASD dc link inductance,  $L_d = 3\% Z_{base}/\omega$ .

ASD line input inductance,  $L_s = 3\% Z_{base}/\omega$ .

ASD output resistance (30% full load),  $R_o = 8.7$  p.u.

Damping resistance,  $R_{damp} = 0.0$  p.u.

Switching power device [=] Toshiba IGBT MG90V2YS40,  $I_c = 90$  A,  $V_{ce} = 1700$  V.

### A. Experimental Setup

Fig. 10 shows the experimental setup. The  $L_s$  and  $C_{sw}$  values are altered to generate a variety of CST events, to which the ASD is subjected in a laboratory setting.

Table I shows the characteristic transient components of the CST events as a function of  $C_{sw}$ .

As  $C_{sw}$  value is changed, the CST natural frequency of oscillation  $f_n$  is altered. Also  $V_{pk}$  and  $V_{pk,crit}$  [as defined in (5) and (6)] are listed.

### B. ASD DC Link Voltage Peak Under a CST Event

The maximum dc link overvoltage transient in the ASD under a CST event is computed from (17). From Fig. 5(a) can be shown a peak voltage close to 4.3 p.u. ( $V_{dc,pk} = 2064$  V). The ASD dc link overvoltage reaches its maximum value in less than half of a cycle (8.33 ms). A commercial ASD could be tripping just at a small percent (25%) above the nominal dc link voltage.

### C. Damping Resistance

In order to mitigate the CST disturbance on the ASD dc link voltage, the proposed approach uses a damping resistance ( $R_{soft-charge}$ ) as shown in Fig. 7. Table II illustrates the

TABLE II  
DAMPING RESISTANCE AT DIFFERENT ASD'S OUTPUT LEVELS TO MITIGATE THE ASD DC LINK OVERVOLTAGE UNDER A CST EVENT

ASD Load (p.u.)	0.1	0.2	0.4	0.6	0.8	1.0
$R_{damp}$ (p.u.)	15.9	7.95	3.98	2.65	1.99	1.6

required damping resistance values,  $R_{damp}$  computed from (27) for different ASDs output levels. The value of the damping resistance  $R_{damp}$  (p.u.), shown in Table II, represents the required effective resistance value to effectively damp the overvoltage ASD dc link voltage caused under a CST event for different ASDs output levels. The electronic damping achieved by the modulation of the semiconductor power device (IGBT) shown in Fig. 7, is suitably adjusted by the control scheme shown in Fig. 8 and given by (28).

## V. SIMULATION AND EXPERIMENTAL RESULTS

Simulation and experimental results for the new method to mitigate nuisance tripping of PWM ASDs due to CST's events are presented in this section.

### A. Simulation Results

As a summary of the simulation results, the proposed approach attempts to mitigate the overvoltage transient in the ASD dc link voltage. Two 480 V, 16 kVA ASDs were simulated which are connected in a typical power distribution system and affected by a utility CST event as shown in Fig. 2. The plot at the top of Fig. 11, shows the CST effect on the utilization bus voltage. This plot illustrates the high overvoltage transient (close to 2 p.u.) and the natural resonance frequency which are dependent on the  $L$ - $C$  parameters of the power system. The middle plot in Fig. 11 shows the dc link voltage for ASD-2 which experiences the overvoltage condition as no mitigation technique is applied. The ASD dc link overvoltage is momentarily increased ( $>1.3$  p.u.) to 1.2 kV. This condition could result in an ASD overvoltage trip due to exceeding the overvoltage trip level. The lower plot in Fig. 11 shows the dc link voltage on ASD-1 when the proposed mitigation technique is applied to reduce or maintain the voltage within nominal or acceptable ASD limits. A simulation of the CST detection circuit, along with an ASD dc link feedback voltage are used to mitigate the momentary dc link overvoltage.

From the simulation results shown in Fig. 11, it can be concluded the feasibility of the proposed approach to mitigate the ASD dc link overvoltage.

### B. Experimental Results

In this section, experimental results for a simulated utility CST event and a commercial 480-V, 16-kVA, 60-Hz ASD are presented. The test setup consists of an ASD equipment powered from a 480-V, 54-kVA programmable ac power source along with a delta-connected capacitor bank. Fig. 10 shows the experiment setup.

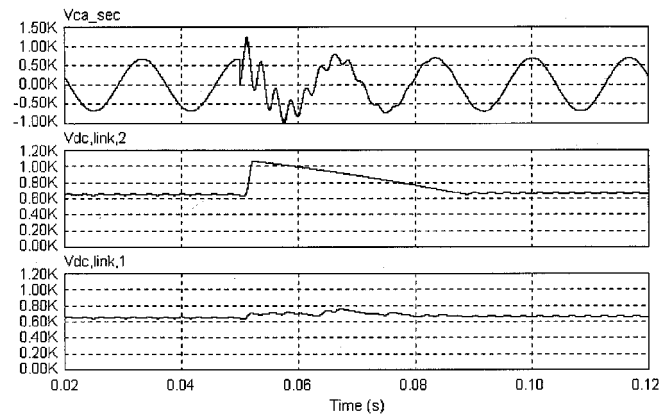
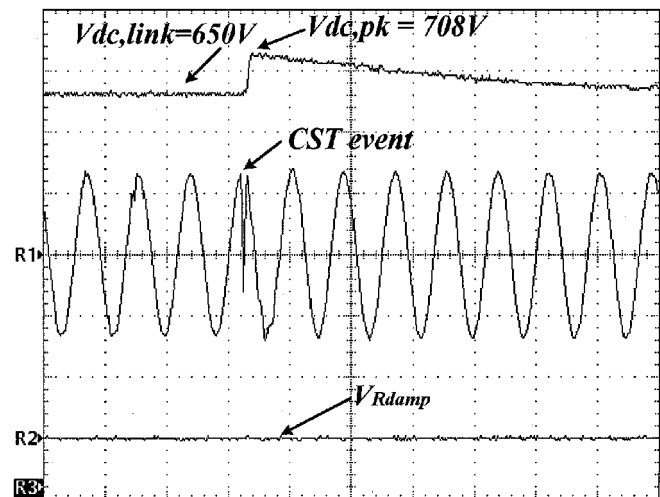
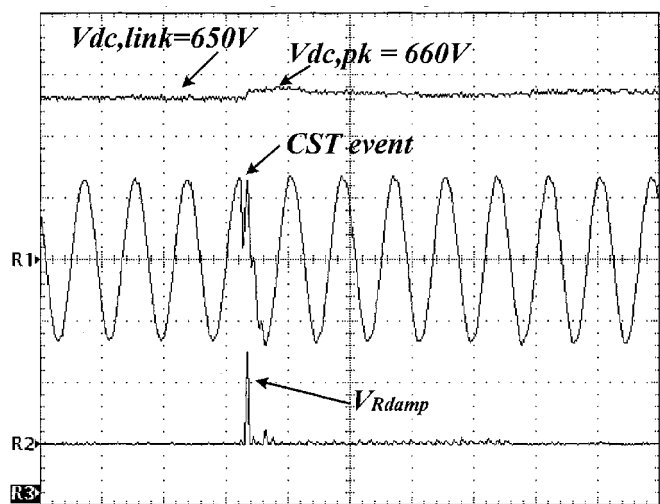


Fig. 11. Simulation results of the proposed approach for two 480-V, 16-kVA ASDs connected in a typical power distribution system.



(a)



(b)

Fig. 12. Experimental results on a 480-V, 16-kVA, 60-Hz ASD equipment with  $C_{SW} = 60 \mu\text{F}$  and  $L_s = 800 \mu\text{H}$  (3%): (a) CST event on ASD without the mitigation approach and (b) CST event on ASD with the mitigation proposed approach. (a) Trace R1: 500 V/div., trace R2: 200 V/div., trace R3: 100 V/div., time base: 20 ms/div. (b) Trace R1: 500 V/div., trace R2: 200 V/div., trace R3: 100 V/div., time base: 20 ms/div.

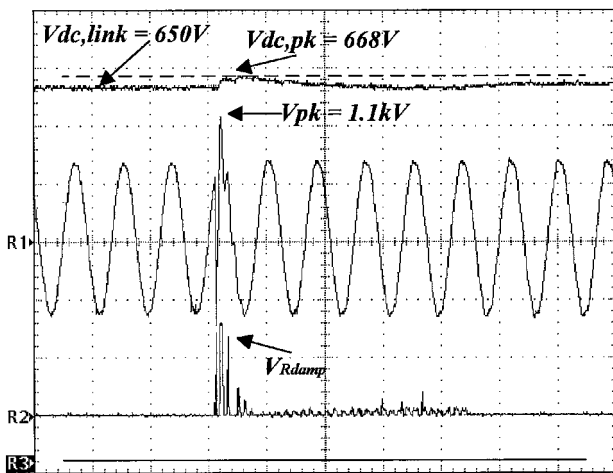


Fig. 13. Experimental results on a 480-V, 16-kVA, 60-Hz ASD equipment with  $C_{SW} = 60 \mu\text{F}$  and  $L_s = 800 \mu\text{H}$  (3%), CST event on ASD with the proposed mitigation approach. Trace R1: 500 V/div., trace R2: 200 V/div., trace R3: 100 V/div., time base: 20 ms/div.

A damping resistance is computed from (27) and explained in Section III, where  $R_{damp} = 76.36 \Omega$ . The ASD equipment embodies a soft-charge resistor, which can be used as the damping resistance. However, the proposed approach achieves the damping effect of the CST event by means of an average damping modulation generated through the soft-charge resistor ( $R_{soft-charge}$ ) along with the integrated IGBT device (Fig. 7).

Fig. 12(a) shows the ASD dc link voltage under a CST event for a 30% ASDs output load without the proposed approach. The dc link increases up to 708 V without tripping the ASD [top trace of Fig. 12(a)]. Fig. 12(b) shows the experimental results with the proposed approach. The top trace in Fig. 12(b) shows the ASD dc link voltage which has been effectively damped due to the proposed approach. The middle and bottom traces in Fig. 12(b) show the line-to-line voltage and the voltage across the soft-charge resistor, respectively.

It is clear, in the bottom trace [Fig. 12(b)], the overvoltage transient generated by the CST event is properly damped across the damping resistance via the pulsewidth-modulated action of the IGBT ( $Q$ ), during the utility disturbance. The momentary high energy generated by the CST event is dissipated in the damping resistance [Fig. 12(b)] during the first half of a cycle at the inception of the CST event. The mitigated action of the proposed approach continues for a five-cycle interval to reduce and maintain the ASD dc link voltage within acceptable limits [Fig. 12(b)].

Fig. 13 shows another experimental result, where it can be illustrated the voltage peak ( $\approx 1.6$  p.u.) of the line-to-line voltage at the inception of a CST event (middle trace, R1). However, the proposed approach helps to mitigate the overvoltage dc link peak voltage ( $V_{dc,pk} = 668 \text{ V}$ ) in the ASD equipment. The lower trace in Fig. 13 shows the damped overvoltage across the damping resistance.

## VI. CONCLUSION

In this paper, a new approach to mitigate nuisance tripping of PWM ASDs due to utility CST events has been proposed.

Simulations and experimental results have shown the feasibility of the new approach to reduce the overvoltage transient in the ASD dc link voltage in order to avoid nuisance tripping. The approach can be easily integrated into ASD equipment as an add-option. The main advantages of the new proposed approach are

- i) electronic damping for CST is achieved by low cost modifications to ASD hardware;
- ii) it adapts to several utility resonance conditions.

A disadvantage for this method would be the cost of the new IGBT-based bypass module in the power flow path of the ASD.

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