

An Approach to Achieve Ride-Through of an Adjustable-Speed Drive With Flyback Converter Modules Powered by Super Capacitors

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Abstract—Adjustable-speed drives under short-term power interruptions can interrupt a critical process. In this paper, an approach to provide ride-through with flyback converter modules powered by super capacitors is explored. The proposed approach is modular and facilitates additional modules to be added to suit higher voltage/power ratings. Both unidirectional and bidirectional flyback dc/dc converter topologies are examined. Simulation and experimental results are presented.

Index Terms—Adjustable-speed drives, power quality, ride-through capability, short-term power interruption, super capacitors.

I. INTRODUCTION

THE application of adjustable-speed drives (ASDs) in commercial and industrial facilities is increasing due to improved efficiency, energy savings and process control. Pulsewidth-modulated (PWM) ASDs feeding induction motors from a constant dc-link voltage have matured as a standard drive technology. However, PWM ASDs are often susceptible to electric power disturbances such as sags, swells, transients, and short-term power interruptions (STPIs), thus resulting in costly nuisance tripping on continuous industrial processes. The dc-link capacitor in an ASD has a relatively small amount

of stored energy. Under an STPI with a duration of 0.5–5 s [1], the dc-link energy is absorbed by the induction motor load within a few milliseconds and nuisance tripping will occur. The resulting nuisance tripping of a continuous industrial process may entail loss or damage of material. This can result in loss in revenue and costly down time. These losses can be avoided for critical production processes by using ASDs with ride-through capabilities [1].

There are a number of approaches that can help to reduce the susceptibility of ASDs to electric power disturbances. The proper selection is based upon the system or process requirements and the cost involved [1]. A variety of energy storage technologies are candidates for providing the needed full-power ASD ride-through under STPIs and sags. Battery backup systems, super capacitors, motor-generator sets, flywheel energy storage systems, superconducting magnetic energy storage (SMES), and fuel cells are some examples of these technologies. Reference [1] presents a comparison of the energy storage characteristics.

In this paper, an approach to achieve ride-through for PWM ASD's under STPIs powered with super capacitors is presented. The proposed approach is modular, i.e., a block of super capacitors is arranged in series and connected to a flyback dc/dc converter to supply energy to the dc link in the event of an STPI. Additionally, a low-power dc/ac inverter is configured as an option to these ASDs, which power their control electronics via input ac power.

A flyback converter topology is shown to be suitable for the short-term ride-through scheme discussed in this paper. A bidirectional flyback converter topology is examined to facilitate quick charging of the super-capacitor modules.

The advantages of the proposed approach include the following.

- 1) The approach can provide ride-through of an ASD for a voltage sag and/or an STPI for 5 s.
- 2) Super capacitors exhibit long life and fast recharge rates.
- 3) The approach requires minimal maintenance.
- 4) The approach is modular and additional super-capacitor/dc-dc converter blocks can be added for higher power ASDs or for longer ride-through times.

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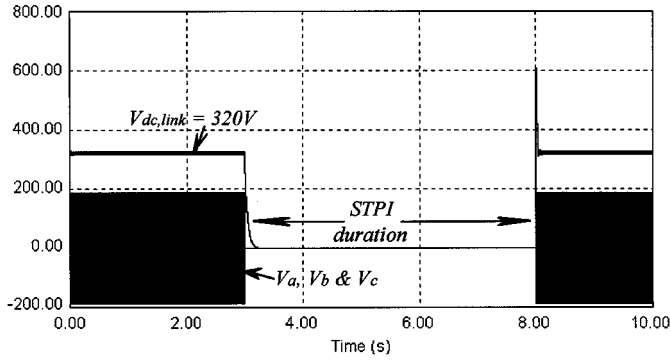


Fig. 1. Simulation results of a 230-V 3-kW ASD under an STPI.

II. EFFECTS OF STPIs ON ASDs

A. DC-Link Voltage Drop Under STPI

An STPI is defined as the complete loss of voltage (<0.10 pu) on one or more phase conductors for a time period between 0.5 cycles and 3 s [2], [3]. STPIs are caused by power system faults, equipment failure, and control malfunction. The duration of an STPI, due to a fault on the utility system, is determined by utility protective devices and the particular event that is causing the fault [3].

An STPI on an ASD can cause some unwanted effects in critical continuous industrial processes. Some processes require that the speed not vary more than 5% and only for 500 ms. Other processes will continue producing an acceptable product even if the speed of the motor drops to 0 r/min, as long as the speed returns to normal after 2 s.

In the event of an STPI, the ASD dc-link capacitor is left to provide all the power to the motor and will quickly drop in voltage. Fig. 1 shows that, for a typical 230-V 3-kW ASD at full load and full speed, it will trip on undervoltage within a few milliseconds.

B. DC-Link Capacitance Requirement Under an STPI

The method of adding capacitors to increase the stored energy needed during ride-through is a simple and rugged approach, but it can provide limited ride-through for smaller loads [1], [4].

However, in the event of an STPI, the amount of stored energy in the ASD dc-link capacitor is normally not sufficient to maintain the normal operation of an ASD in a critical continuous process. The ASD power is drawn from the dc-link capacitor C_d . Hence, there is a maximum duration in the interval of an STPI before an ASD nuisance tripping may occur. The maximum duration t_m is determined by solving

$$\int_{t_{\text{int}}}^{t_{\text{trip, level}}} P_d(t) dt = \frac{1}{2} C_d [V_{\text{dc, nom}}^2 - V_{\text{dc, trip}}^2] \quad (1)$$

where t_{int} represents the time when the STPI is initiated and sensed, and $t_{\text{trip, level}}$ is the time when the ASD dc-link voltage reaches a predetermined voltage level (trip level). $V_{\text{dc, nom}}$ is the nominal average value of the dc-link voltage and $V_{\text{dc, trip}}$ is the predetermined dc-link voltage trip level.

From the widely publicized Computer & Business Equipment Manufacturers Association (CBEMA) curve [5], [6], which defines typical computer tolerance to voltage variations, the minimal threshold value of the input voltage in order to maintain the operation of critical equipment under electric disturbances is 0.87 p.u. Although specific critical process equipment designs (e.g., ASDs) do not necessarily match the exact minimal and maximum thresholds of the CBEMA curve, it is a widely recognized consensus curve. A typical ASD is set to trip when the drop in the ASD dc-link voltage $V_{\text{dc, link}}$ is 0.87 times the nominal value. For a 230-V, 60-Hz, and 3-kW ASD, the dc-link voltage for continuous operation is given by

$$V_{\text{dc, link}} = 1.35 * V_{LL} = 310 \text{ V}. \quad (2)$$

Therefore, a dc-link voltage trip level is computed from (2) as $V_{\text{dc, trip}} = 0.87V_{\text{dc, link}} = 270 \text{ V}$.

The average dc-link current, I_{dc} , for a 3-kW (P_o) motor load is given by

$$I_{\text{dc}} = \frac{P_o}{V_{\text{dc, link}}} = 9.68 \text{ A}. \quad (3)$$

A typical 3-kW PWM ASD [23] utilizes a 1000- μF dc-link capacitor to filter and maintain a constant dc-link voltage. Now, the ASD under an STPI must be powered exclusively by the dc-link capacitor C_d . The maximum ride-through duration for the dc-link capacitor for powering the ASD before a trip may occur can be computed from (1)

$$t_m = \frac{1}{2} C_d \frac{V_{\text{dc, nom}}^2 - V_{\text{dc, trip}}^2}{P_o} = 3.87 \text{ ms}. \quad (4)$$

The time $t_m = 3.87 \text{ ms}$ would be the duration to discharge the 1000- μF dc-link capacitor from 310 to 270 Vdc. This time translates into 1/3 of a cycle at 60-Hz frequency. Thus, 1000 μF on the dc link can only provide a full-power ride-through of a 3-kW ASD for 1/3 of a cycle. If the STPI were to last, at the worst case, for 5 s (i.e., $t_m = 5 \text{ s}$, 300 cycles) the capacitance required to provide the ASD ride-through can be computed as

$$C = I \frac{dt}{dV} \quad (5)$$

$$C = \frac{I_{\text{dc}} * t_m}{V_{\text{dc, nom}} - V_{\text{dc, trip}}} = \frac{9.68 * 5}{310 - 270} = 1.21 \text{ F}. \quad (6)$$

The resulting capacitance of 1.21 F clearly shows that additional 1210 \times 1000 μF capacitors would have to be added to the dc link in order to reach a total of 1.21 F. Each 1000- μF capacitor is rated at 400 Vdc. A bank of 1210 \times 1000 μF capacitors should be connected in parallel to the dc link. This method would bring the following disadvantages:

- additional hardware and space requirements;
- new circuit consideration on charging and discharging the additional dc-link capacitor bank;
- high cost.

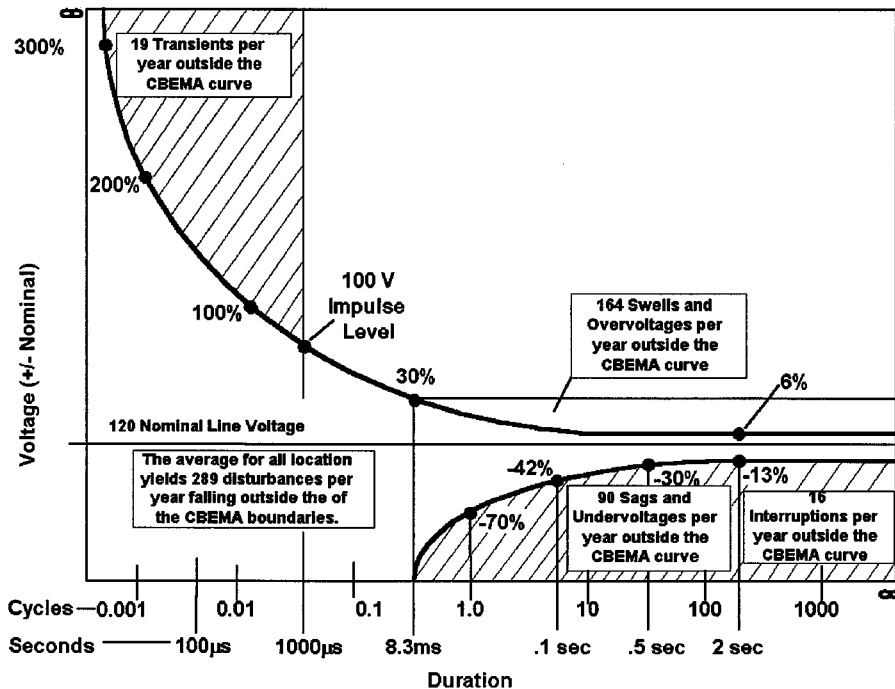


Fig. 2. Power quality events outside the CBEMA curve.

Furthermore, the cost of enclosure, fuses, bus bars, and precharging circuits would be additional.

C. STPI Cost Analysis

Power quality disruptions currently cost U.S. companies more than \$25 billion annually [2], [7]–[9]. Some examples of costly critical power quality situations include: interruptions to semiconductor batch processing costing \$3000 to greater than \$1 million per incident; an STPI at an automobile manufacturing plant costing over \$300 000 with reported losses of \$15 000/min; an STPI of just 5 cycles (83 ms) costing a glass plant \$200 000 [2], [7]–[9].

It is shown in [2], that these losses can be avoided for critical production processes by using ASDs with ride-through capabilities.

In order to determine whether or not applying PWM ASD ride-through capability will be cost effective, STPI costs can be estimated.

Power quality and power interruption cost surveys have been performed in the last 12 years by utilities in the U.S. and Canada [3], [5], [7], [10], [11]. The information collected from these surveys provides a detailed picture of the expected electrical environment in which ASDs are intended to operate. In the surveys performed in [5] and [10], data were collected with the following voltage event types: sag, swell, overvoltage, undervoltage, impulse, transient surge, and interruptions (outages). In Fig. 2, the range of events that might be expected at the majority of locations is visually shown.

Fig. 2 shows the results of applying the CBEMA curve limits to the collected data. As indicated, an average of 289 disturbances fall outside the CBEMA boundaries per site, per year. This includes 19 transients, 164 swell or overvoltage conditions, and 16 interruptions. Other sites are shown to experience zero

disturbances, while the worst locations experienced 7121 sags and 146 interruptions, [5].

As expected, the majority of the events exceeding the CBEMA limits are just beyond the thresholds of the curve.

Fig. 3 shows the results from the survey reported in [12] and [13]. The information shown in Fig. 3 is presented to relay power disturbances in the form of rms voltage variations. The height of each column corresponds to an incidence rate for a particular voltage magnitude and duration pair.

The power quality surveys include comprehensive statistical data of STPI (momentary interruption) costs which are carried out by some utilities mentioned in [7]. Thus, using statistics of average annual events, industry customers can predict downtime costs and make comparisons with the cost of additional ASD ride-through capability.

III. USE OF SUPER CAPACITORS FOR ASD RIDE-THROUGH

In the recent past, super capacitors have emerged as viable energy storage devices [15], [17]. Super capacitors possess a number of unique characteristics that enable their utilization in a wide range of applications (e.g., hybrid electric vehicles/electric vehicles (HEVs/EVs), uninterruptible power supply (UPS) systems, ASD ride-through applications). Some of these features include the following:

- energy densities 100 times greater than conventional capacitors;
- power densities 10 times greater than conventional batteries;
- specific energy range of 1.12–2.48 Wh/kg;
- charge and discharge times from fractions of a second to several minutes;
- rated capacitance range of 0.043–2700 F;

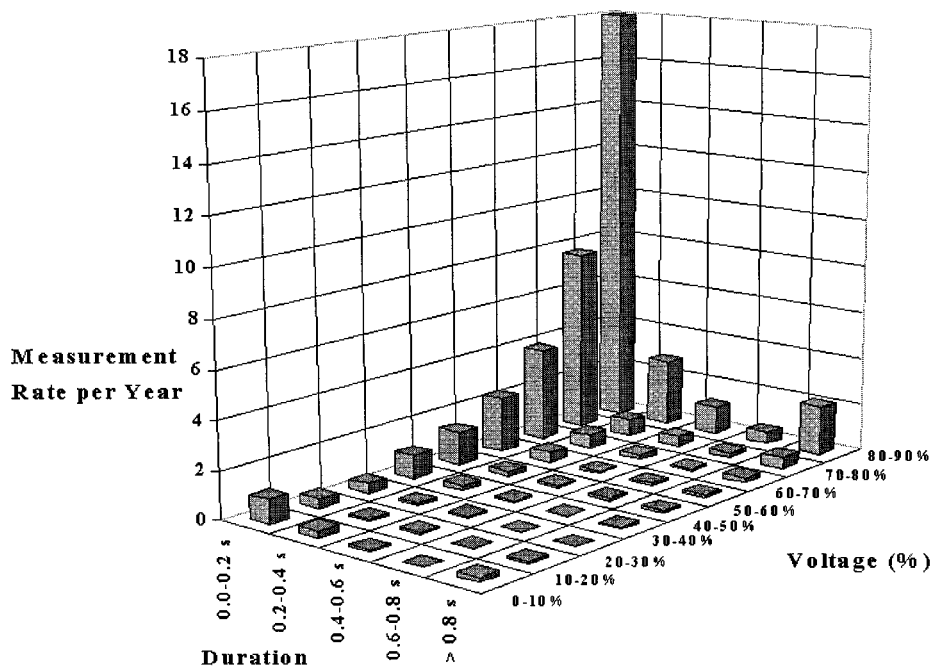


Fig. 3. Magnitude and duration of rms voltage variation.

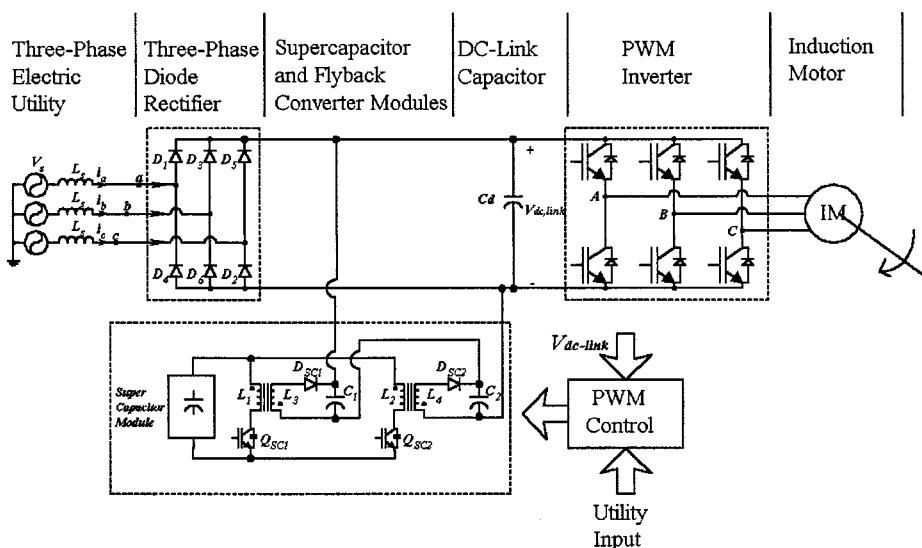


Fig. 4. Proposed ASD ride-through approach with super-capacitor module and FBCMs.

- nominal voltage ranging from 2.3 to 100 V;
- rated current ranging from 3 to 600 A.
- power range 5–100 kW;
- cycle life greater than 100 000;
- operating temperature range of $-20\text{ }^{\circ}\text{C}$ – $55\text{ }^{\circ}\text{C}$;
- modular and stackable;
- lowest cost per farad;
- maintenance-free operation;
- environmentally safe.

The capabilities listed above offer to meet the electric power demands required in some power quality applications. In ASD ride-through applications, super capacitors are capable of quick discharge and, hence, are suitable for transient ride-through of ASDs under sags and STPIs.

IV. PROPOSED RIDE-THROUGH APPROACH

A. ASD Ride-Through With Flyback Converter Module (FBCM) and Super Capacitors

Fig. 4 shows the proposed ride-through approach to provide ride-through capability to an ASD under STPI. The proposed ride-through approach consists of one super capacitor module connected in shunt to the dc link of the ASD through dc-dc converters. The super-capacitor module provides the energy to the dc link via the operation of a pair of flyback converter modules (FBCMs) operating at a high frequency.

The outputs of the flyback converters are connected in series to further increase the voltage and be compatible with the ASD dc link. The insulated gate bipolar transistors (IGBTs) (Q_{SC1}

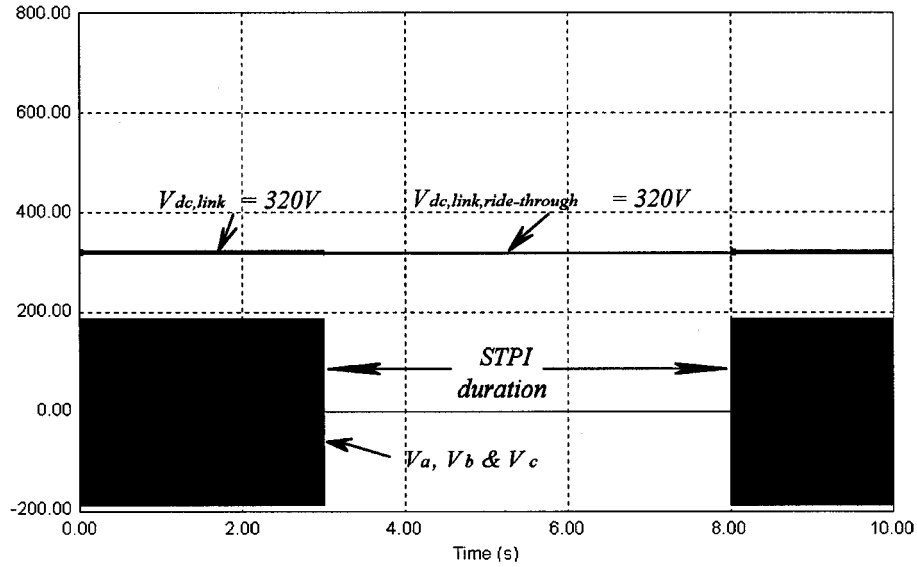


Fig. 5. Simulation results on a 230-V 3-kW ASD for an STPI with the proposed FBCM and super-capacitor ride-through approach.

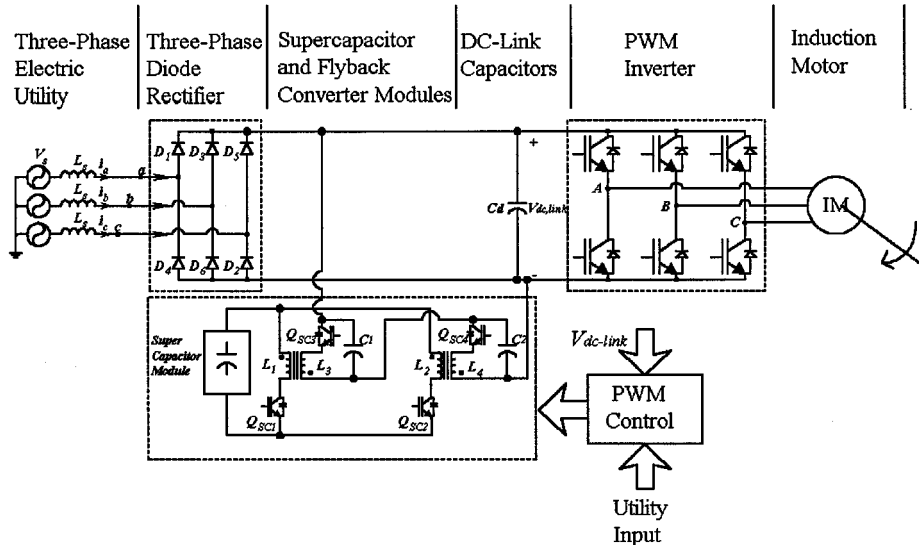


Fig. 6. Proposed ride-through approach with bidirectional dc/dc flyback converters to facilitate charging and discharging of super-capacitor modules.

and Q_{SC2}) are turned on/off at a constant switching frequency (f_s). The switch duty cycle is varied in the event of an STPI detection. During the on time, energy is stored in the primary coupled inductors (L_1 and L_2). During the off time, the induced energy on the secondary coupled inductors (L_3 and L_4) is transferred to the dc link through diodes (D_{SC1} and D_{SC2}).

Fig. 5 shows the operation (simulated) of the proposed ride-through approach under an STPI of 5-s duration. Notice the dc-link voltage being maintained for the entire duration of the STPI.

The design example illustrates the selection of inductor turns ratio and component values associated with the flyback converter.

B. ASD Ride-Through With Bidirectional FBCMs and Super Capacitor

Fig. 6 shows an alternative topology consisting of a bidirectional flyback converter to ride-through under an STPI and also

charge the super-capacitor modules during normal conditions. Hence, as described previously, the super-capacitor module along with modified FBCMs would transfer energy to the dc link in the event of an STPI. The IGBTs (Q_{SC1} and Q_{SC2}) are turned on/off adequately, whereas IGBTs (Q_{SC3} and Q_{SC4}) remain inactive. Under normal conditions (i.e., not an STPI event) or even at lighter loads, IGBTs (Q_{SC3} and Q_{SC4}) would be turned on/off to charge the super-capacitor modules from the dc link at a constant frequency. The IGBTs (Q_{SC1} and Q_{SC2}) would remain inactive under this operation.

C. Feedback Control Loop of FBCMs

Fig. 7 shows the electronic control circuit of the proposed approach. The dc-link voltage of the ASD is sensed via a resistor network as shown in Fig. 7. A feedback voltage V_{fb} is derived from the resistor network and serves as the input voltage to an isolation amplifier [18]. The feedback voltage is adequately conditioned, filtered, and postamplified by the isolation am-

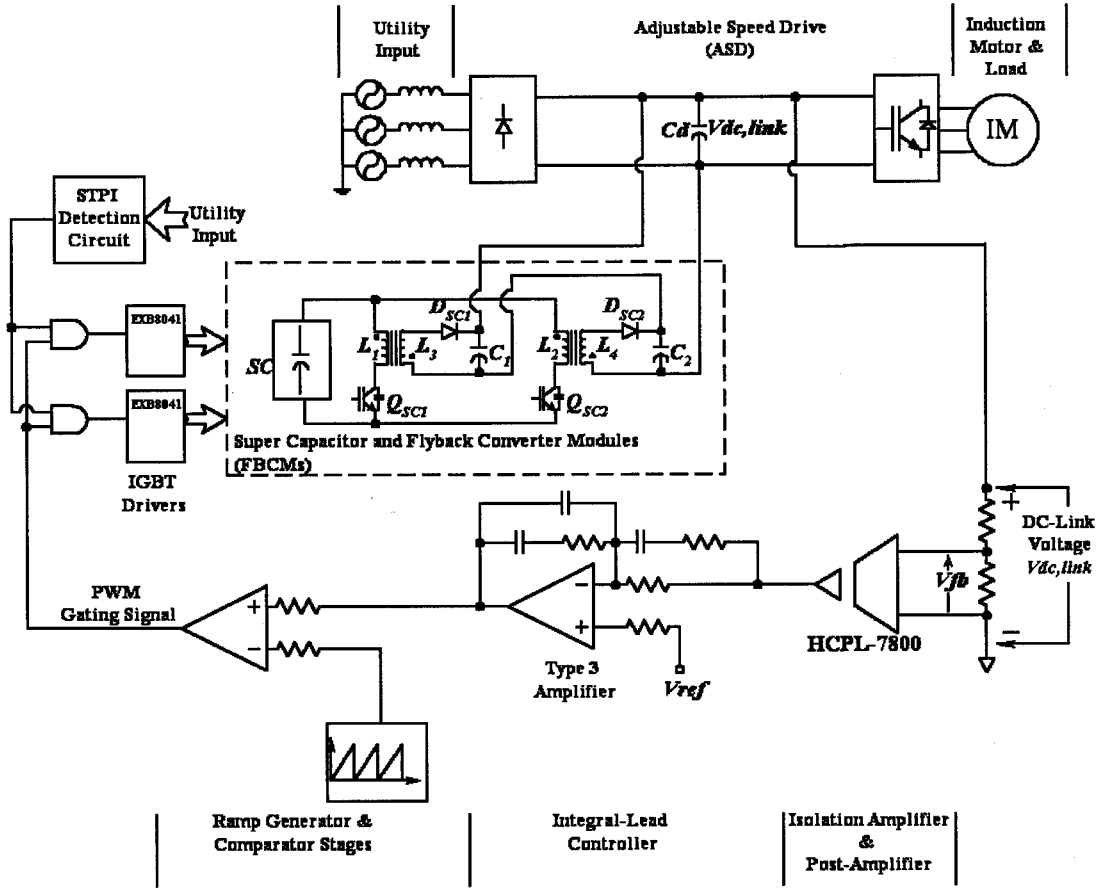


Fig. 7. Electronic feedback control circuit.

plifier (HCPL-7800) and a differential amplifier, respectively. Thus, an accurate feedback voltage signal is produced from the dc-link voltage of the ASD.

A type-3 amplifier [19]–[21] or integral-lead controller [22] is then used to apply feedback control loop to the FBCMs operating in discontinuous conduction mode. The PWM gating signal to drive the FBCMs is properly controlled by this feedback loop technique. A proper evaluation of the loop gain of the entire system served to provide the essential information of the FBCMs, sensing, and controller circuits in order to design for the best performance of an ASD under STPI.

Fig. 8 shows a block diagram of the feedback control system of the FBCMs. In this figure, $T_c(s)$ represents a transfer function of the controller, $T_m(s)$ represents a transfer function of the modulator, and $T_p(s)$ represents the control-to-output voltage transfer function of the power stage (FBCMs).

Also shown in Fig. 8 is the feedback network β , along with the isolation amplifier gain, which are used for sampling the ASD dc-link voltage $V_{dc, link}$.

The open-loop transfer function for the FBCMs is defined by

$$T_{OL}(s) = \beta T_m T_p(s) T_c(s). \quad (7)$$

In Fig. 8, the transfer function $T_c(s)$ represents a compensated error amplifier also known as an integral-lead controller.

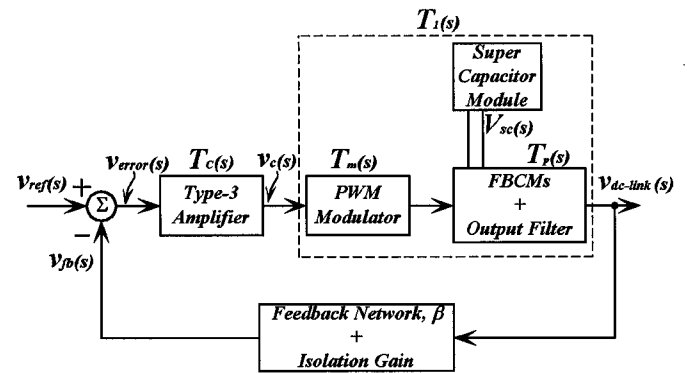


Fig. 8. Block diagram of the feedback control system of the FBCMs.

The transfer function $T_c(s)$ must be properly tuned so that $T_{OL}(s)$ meets the performance requirements to minimize the steady-state error in the ASD dc-link voltage under an STPI. Furthermore, the controller must reduce the sensitivity of the closed-loop gain $|T_{CL}(s)|$ to component values over a wide frequency range. It must also achieve a fast transient response to sudden changes in the super-capacitor voltage, V_{SC} , or the ASD output load. Moreover, sufficient gain margin (GM) (6–12 dB), and phase margin (45° – 60°) must be achieved. References [19]–[22] give the foundation for the design of the type-3 amplifier circuit.

V. DESIGN EXAMPLE

Figs. 4 and 6 show the proposed FBCMs powered by super capacitors. Currently available super capacitors from Maxwell are rated at 2700 F at 2.3 V. Connecting 28 cells in series, one can realize a 56-V 96-F module with 150 kJ of stored energy capacity.

A. Calculation of Energy Storage Requirement for ASD Ride-Through

$$\begin{aligned} \text{Utility rms voltage} &= V_{LL} \\ \text{dc-link voltage, } V_{\text{dc link}} &= 1.35V_{LL} \\ \text{ASD power rating} &= P_{\text{ASD}} \\ \text{STPI duration} &= t_{ri} \\ \text{energy stored in the super-capacitor module} &= E_{\text{SC}} = \\ &= (1/2) CV_{\text{SC}}^2 \end{aligned}$$

where “ C ” is the capacitance and V_{SC} is the voltage rating of the super-capacitor module.

Since the energy stored in a super capacitor is a direct function of the voltage, a drop in 30% voltage (V_{SC} to $0.7 V_{\text{SC}}$) represents the release of 50% of the stored energy. Further, losses in the power converters (FBCMs) and the losses in the super-capacitor resistance (ESR) also need to be accounted for. Adopting this discharge strategy, the following equation can be written:

$$\frac{1}{2} [CV_{\text{SC}}^2 - C(0.7V_{\text{SC}})^2] * \eta = P_{\text{ASD}} * t_{ri} \quad (8)$$

where η represents the efficiency for the FBCMs and the super-capacitor module.

For an example, a 230-V 15-kW ASD load employing a 56-V 96-F super-capacitor module with the proposed FBCMs, and $\eta = 0.9$ (90% efficiency), t_{ri} can be computed as follows:

$$\begin{aligned} V_{\text{SC}} &= 56 \text{ V} \\ C &= 96 \text{ F} \end{aligned}$$

then

$$t_{ri} = 4.61 \text{ s.}$$

Therefore, 4.61-s ride-through can be achieved.

B. FBCM Design

Flyback converter topology is suitable for a short-term ride-through scheme since it employs fewer power semiconductor devices. Also, isolation and high transfer ratio are necessary. These requirements make the flyback converter more suitable for this application.

In the approach shown in Fig. 4, the output stages of the FBCMs are connected in series to power the ASD dc link. The input/output relationship for FBCMs (Fig. 4) is

$$\frac{V_{\text{out}}}{V_{\text{in}}} = \frac{V_{\text{dc link}}}{2 * V_{\text{SC}}} = \frac{N_2}{N_1} \frac{D}{1-D} \quad (9)$$

where N_2/N_1 is the turns ratio of the boost inductor and D is the PWM duty cycle.

For a 230-V 3-kW ASD, $V_{\text{dc link}} = 1.35 * 230 \text{ V} = 310 \text{ V}$. Selecting a turns ratio $N_2/N_1 = 3$, and $1 \text{ p.u.} \leq V_{\text{SC}} \leq 0.7 \text{ p.u.}$

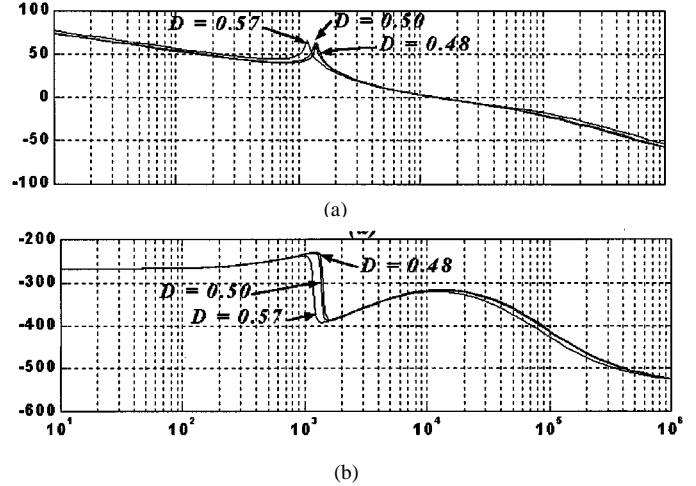


Fig. 9. Bode plots of the transfer function $T_{\text{OL}}(s)$, for the open-loop FBCM system. (a) Magnitude $|T_{\text{OL}}(s)|$ (dB) versus frequency (rad/seg). (b) Phase $\phi_{T_{\text{OL}}}$ (degrees) versus frequency (rad/seg).

From (9), we have

$$0.48 \leq D \leq 0.569.$$

C. Type-3 Amplifier Design

The design procedure of the type-3 amplifier is as follows. A crossover frequency of $f_{\text{cross}} = (1/4)f_s = 2.5 \text{ kHz}$ is assumed. That is, $\omega_{\text{cross}} = 1.57 \times 10^4 \text{ rad/s}$, where $f_s = 10 \text{ kHz}$.

From Bode plots of the transfer functions $T_1(s)$ and $T_P(s)$, (Fig. 8), at the selected crossover frequency, we have,

$$\phi_{T_P} = \phi_{T_1} = -188^\circ.$$

A phase margin is assumed $PM = 45^\circ$ and duty cycle interval is defined from (9) as $0.48 \leq D \leq 0.57$.

The component values for the type-3 amplifier are computed as described in [19]–[22].

Fig. 9 shows the Bode plots for the transfer function of the open-loop FBCM system, $T_{\text{OL}}(s)$. Fig. 9(a) shows the magnitudes $|T_{\text{OL}}(s)|$ in decibels for three different duty cycles (D_{min} , D_{nom} , and D_{max}). Fig. 9(b) shows the phase $\phi_{T_{\text{OL}}}$ in degrees, as a function of frequency for three different duty ratios.

Fig. 10 shows the Bode plots for the transfer function of the closed-loop FBCM system $T_{\text{CL}}(s)$, for three different duty cycles (D_{min} , D_{nom} , and D_{max}). Fig. 10(a) shows the magnitude $|T_{\text{CL}}(s)|$ in decibels and Fig. 10(b) shows the phase $\phi_{T_{\text{CL}}}$ in degrees, as a function of frequency. The gain at low frequencies is 40 dB. It is shown [Fig. 10(a)] that the crossover frequency is roughly $\omega_{\text{cross}} = 3 \times 10^5 \text{ rad/s}$ for the three magnitude plots. The phase shift (boost) produced by the controller is observed at $\omega_{\text{cross}} = 1.57 \times 10^4 \text{ rad/s}$ [Fig. 10(b)].

VI. EXPERIMENTAL RESULTS

In this section, experimental results are presented. A 56-V dc power supply is used in place of super-capacitor modules. A three-phase short-term power interruption is generated by

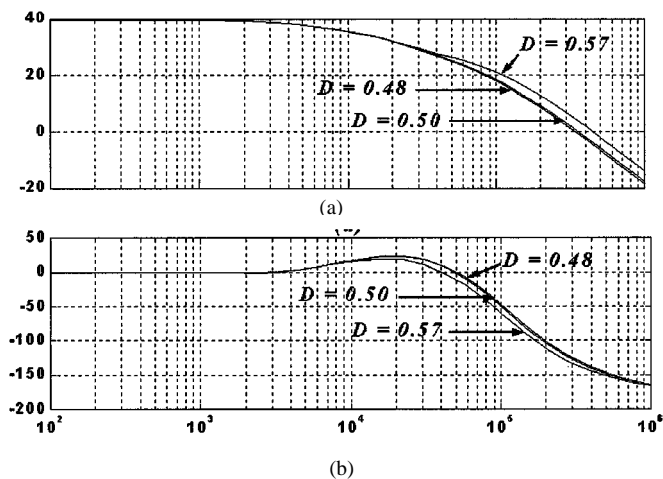


Fig. 10. Bode plots of the transfer function $T_{CL}(s)$ for the closed-loop FBCM system. (a) Magnitude $|T_{CL}(s)|$ (dB) versus frequency (rad/seg). (b) Phase $\phi_{T_{cl}}$ (degrees) versus frequency (rad/seg).

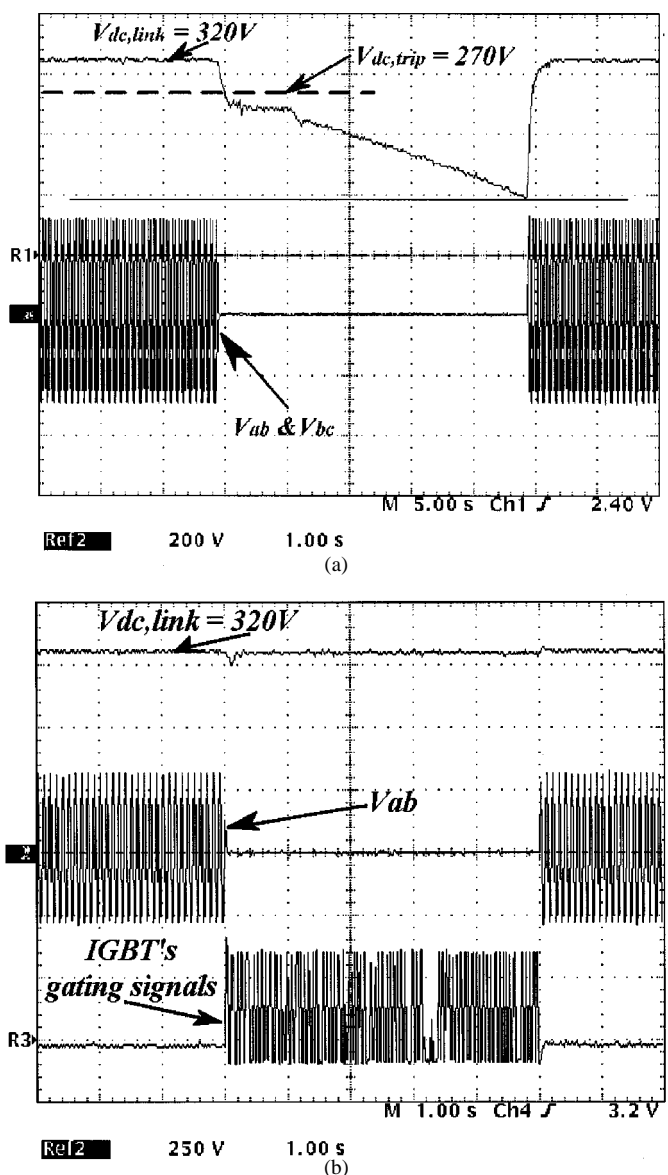


Fig. 11. Experimental results on a 230-V 3-kW ASD for an STPI. (a) No ride-through option. (b) With the proposed super-capacitor ride-through approach.

a 480-V 54-kVA programmable ac power source. The programmable ac power source facilitates the generation of a wide variety of transient and steady-state power quality disturbances. Fig. 11 shows results obtained on a 230-V 3-kW ASD under no-load condition. Fig. 11(a) shows the decay of the dc-link voltage under an STPI of 5 s. Fig. 11(b) shows the variation of the dc-link voltage with the FBCMs in operation. The dc-link voltage is maintained by the FBCMs along with the feedback control loop system.

VII. CONCLUSIONS

In this paper, an approach to achieve ASD ride-through with FBCMs powered by super capacitors has been presented. A modular design of FBCM is explored. A design example has been shown to aid calculations. The ASD dc-link voltage is effectively maintained at its nominal value under an STPI. The feedback control loop was designed to have a phase margin equal to 45° . An optimal condition should avoid a minimal phase shift below 45° . Simulation and experimental results have demonstrated the feasibility of the proposed approach.

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