An Integrated Single-Switch Approach to Improve Harmonic Performance of Standard PWM Adjustable-Speed Drives

Steffan Hansen, *Member, IEEE*, Prasad N. Enjeti, *Fellow, IEEE*, Jae-Hong Hahn, *Student Member, IEEE*, and Frede Blaabjerg, *Senior Member, IEEE*

***Abstract*—In this paper, an integrated single-switch approach to improve harmonic performance of standard pulsewidth modulation adjustable-speed drives (ASD's) is presented. The approach is essentially an add-on solution to a standard ASD topology. The approach is based on circulating a third harmonic current to reduce the harmonics of the line current. The dynamic braking chopper available in standard ASD's is used to control the amplitude of the third harmonic circulating current. Analysis, design, and simulations are presented to determine the performance of the proposed scheme with different line impedance and with and without dc-link inductance in the ASD. Utility input current distortion well below 15% is obtained. This paper also presents how this new approach is capable of reducing the harmonic distortion in multiple drives. The paper includes experimental results using a 480-V 10-kW commercial ASD retrofitted with the proposed approach.**

***Index Terms*—Adjustable-speed drive, harmonic distortion, power quality, rectifiers, third harmonic injection.**

I. Introduction

THE expanding use of electric loads controlled by power electronics such as PC's, TV's, stereos, and adjustable-speed drives (ASD's) has made power converters an important and unquestionable part of modern society. Nevertheless, the increasing use of power converters has also led to an increase of current harmonics drawn from the utility grid.

In the last decade, major focus has been on harmonic reduction techniques and, as a result of this, several useful harmonic reduction techniques exist for the single-phase rectifier. However, finding the right solution for the three-phase rectifiers is still very difficult. This seems to be true especially for industrial ASD's where the price and reliability have the highest priorities. Even though there exist many proposals for the three-phase rectifier, many of the existing solutions may not be qualified for a grade-purpose ASD. The solution is either only practical for low-power applications or the price and complexity are too high. Some summaries on three-phase harmonic reduction techniques can be found in [1]–[5].

So far, most customers of ASD's use the low-cost diode rectifier and accept the harmonic currents. Harmonic reduction equipment such as an active filter or active rectifier is only used when there are severe problems with harmonic distortion. Due to the new standards, such as IEEE 519-1992 and EN 61000-3-2/EN 61000-3-12, a more general solution is desired for the ASD.

Some requirements for the three-phase rectifier used for ASD's are as follows.

- The harmonic distortion of the input current should be as low as possible. However, a unity power factor is not necessary.
- There should be no increased dc-link voltage, because higher dc-link voltage warrants redesign of the pulsewidth modulation (PWM) inverter.
- The operation of the rectifier should be independent of the line impedance.
- No additional components in series with the power flow path should be used, due to increased losses.
- Bidirectional power flow is normally not necessary.
- In general, an electrical isolation between the utility input and the output of the power electronic converter is not needed.
- The cost, power losses, and size compared to the diode rectifier should be as small as possible.

Note that the only requirement limiting the use of the diode rectifier is the first requirement in the list above.

The third harmonic injection scheme for the three-phase diode rectifier for reducing the harmonic currents has shown some promising results and has been presented among others in [6]–[10].

However, these approaches suffer from some disadvantages.

- The schemes in [6] and [7] need a line-synchronized controllable external third harmonic current source.
- These schemes also need an input transformer with access to the neutral terminal for circulating the third harmonic current.
- The schemes in [9] and [10] have two diodes in series with the power flow path which increases the losses.

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S. Hansen is with Danfoss Drives A/S, DK-6300 Graasten, Denmark (e-mail: s_hansen@danfoss.com).

P. N. Enjeti and J.-H. Hahn are with the Power Electronics and Power Quality Laboratory, Department of Electrical Engineering, Texas A&M University, College Station, TX 77843-3128 USA (e-mail: enjeti@tamu.edu; jaehong@ee.tamu.edu).

F. Blaabjerg is with the Institute of Energy Technology, Aalborg University, DK-9220 Aaalborg East, Denmark (e-mail: fbl@iet.auc.dk).

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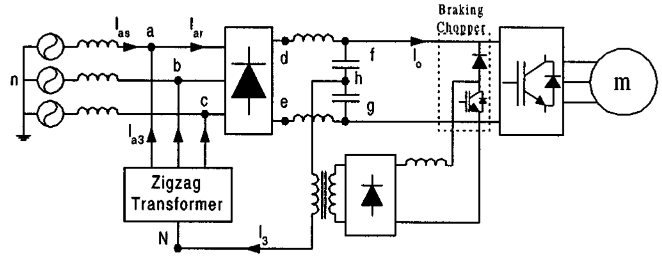

Fig. 1. Proposed integrated single-switch approach to improve harmonic performance of standard adjustable-speed drives.

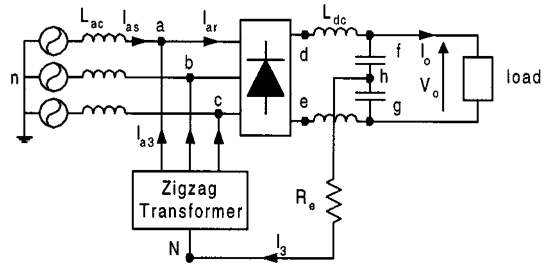

Fig. 2. Simplified diagram of the proposed scheme showing the basic idea.

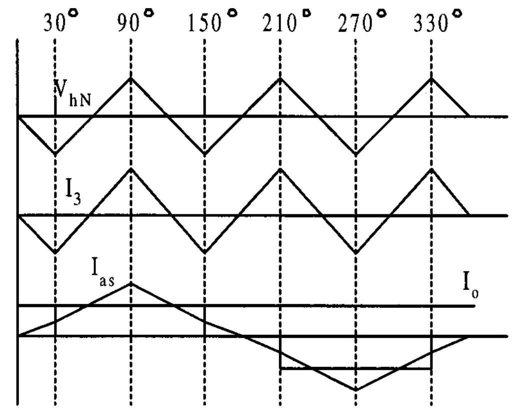

Fig. 3. The voltage V_{hN} between the dc-link midpoint "h" and the neutral "N". The current I_3 is in phase and shape with the voltage. The line current I_{as} can be reconstructed as a function of the dc-link output current I_o and the circulating third harmonic current I_3.

- These schemes also have a high dc-link voltage due to the boost operation and, therefore, increase the losses of the PWM inverter.

The scheme presented in [8], compared to [9] and [10], exhibits the following advantages.

- There are no additional components in series with the power flow path.
- The dc-link voltage is the same as for the diode rectifier.
- The third harmonic circulating current is automatically generated.

However, the scheme in [8] is most suitable for a rectifier with a high dc-link inductance and small dc-link capacitors (e.g., dc motor drives). Furthermore, the circulating third harmonic current is uncontrolled and the optimum total harmonic distortion (THD) is valid only at one operating point.

In this paper, an extension of the scheme in [8] is presented, where the principal of operation basically is the same as in [8]. However, by employing an integrated single-switch boost converter in the scheme, it becomes suitable for improving the harmonic performance of a standard PWM-ASD. The new aspects of this paper are: 1) analysis of the modified scheme of [8] applied to a standard PWM-ASD and 2) effective control of the circulating current. Furthermore, in Section IV, it is shown how the proposed approach is capable of reducing the line-side harmonic currents of multiple ASD's.

The paper includes a detailed design procedure along with component ratings. Detailed simulation and experimental results are also shown.

II. Proposed Topology

Fig. 1 shows the circuit topology of the proposed scheme. In this paper, a zigzag transformer is employed to create a neutral "*N*." Further, a single-phase transformer is connected between "*N*" and the dc-link mid-point "*h*." On the secondary side of the single-phase transformer a single-phase boost power-factor-correction circuit is implemented as shown in Fig. 1. Since the voltage between "*N*" and "*h*" is predominantly 180 Hz (third harmonic), the single-phase boost converter action results in thirrd harmonic injected current I_3 and drastically improves the utility power quality performance of the ASD. It should be noted that the dc-link capacitor midpoint and a dynamic braking chopper (insulated gate bipolar transistor (IGBT) and diode) exist in most standard ASD's.

The advantages of the proposed scheme (Fig. 1) are the following.

- No additional components in the power flow path are needed.
- The dc-link voltage has the same level as with a diode rectifier.
- The operation of the new scheme is independent of the line impedance.
- The approach is an add-on solution. (Once the ASD is modified for the presented scheme, the ASD can easily be sold with the proposal if required.)
- It has high reliability because the diode rectifier still works even when the boost rectifier is down.
- Using the diode and the IGBT of the dynamic braking circuit, low cost can be achieved.
- Multiple drive connection is possible.

III. Principle of Harmonic Reduction with the Proposed Scheme

For description of the proposed scheme, the simplified diagram of Fig. 2 is used, since the boost converter behaves like a variable resistor.

As shown in Fig. 3 the shape of the voltage V_{hN} between the dc-link midpoint 'h' and the neutral of the zigzag transformer "N" is triangular in nature due to the 120° conduction mode of the six-pulse diode rectifier. Interconnection between point "h" and point "N" via a resistor R_e results in a circulating current I_3, in shape and phase with the voltage V_{hN}. This circulating current is essentially a third harmonic current and is injected into the three phases "a," "b," and "c" via a zigzag transformer.

In each phase, a third of the circulating current is injected. Depending of the conduction mode of the six-pulse diode rectifier, three different modes are considered for each phase. For phase "a," these three modes are described below.

Mode 1: Phase "a" is not conducting. In this case, a third of the circulating current I_3 is injected into the source. The source current of phase "a", I_{as}, equals

$$I_{as} = -\frac{I_3}{3}. \quad (1)$$

Mode 2: This is the positive conduction mode. The upper diode of phase "a" in the six-pulse diode rectifier is conducting. Half of the circulating current is flowing into the rectifier via phase "a." The other half is flowing into the rectifier via the lower diode of phase "b" or "c." The upper diode of phase "a" is also conducting the load current into the rectifier. Therefore, the source current of phase "a," I_{as}, equals

$$I_{as} = I_o + \frac{I_3}{2} - \frac{I_3}{3} = I_o + \frac{I_3}{6}. \quad (2)$$

Mode 3: This is the negative conduction mode. The lower diode of phase "a" in the six-pulse diode rectifier is conducting. Half of the circulating current is flowing into the rectifier via phase "a." The other half is flowing into the rectifier via the upper diode of phase "b" or "c." The lower diode of phase "a" is also conducting the load current back to the source. Therefore, the source current of phase "a", I_{as}, equals

$$I_{as} = -I_o + \frac{I_3}{2} - \frac{I_3}{3} = -I_o + \frac{I_3}{6}. \quad (3)$$

The source current can now be reconstructed as shown in Fig. 3. A detailed description of the principles of the third harmonic injection scheme can be found in [8].

In a standard PWM-ASD, the harmonic content of the input current depends both on the dc-link inductance and the ac-line reactance. However, the input current seldom has a square-wave form as assumed in the description above. In some cases, the input current can be discontinuous. Therefore, finding the optimal amplitude of the circulating current that results in the lowest current THD in an analytical way is quite cumbersome. In this paper, the SABER simulator is used for the analysis part. The analysis is based on per-unit quantities with the following definitions:

$$\begin{aligned}\text{input line–line voltage } V_{ab} &= 1 \text{ per unit}\\ \text{output power } P_o &= 1 \text{ per unit}\\ \text{rectifier output dc voltage } V_o &= 1.35 \text{ per unit}\\ \text{output dc current } I_o &= P_o/V_o = 0.7407 \text{ per unit}\\ \text{base impedance } Z_b &= V_{ab}^2/P_o = 1 \text{ per unit.}\end{aligned}$$

The scheme of Fig. 2 is implemented in SABER. The capacitor banks in the dc link equal 10.5% (percentage of the base impedance as defined above). The simulations are done with and without a 2.6% dc-link inductance. The frequency is 60 Hz and the ac impedance is varied, i.e., the short-circuit ratio R_{sc} is varied from 20 to 500. The short-circuit ratio is defined as the ratio between the short-circuit power S_{sc} at the point of connection and the fundamental input power of the ASD S_1. After a total of 90 simulations to analyze the input current THD, the results are shown in Figs. 4 and 5.

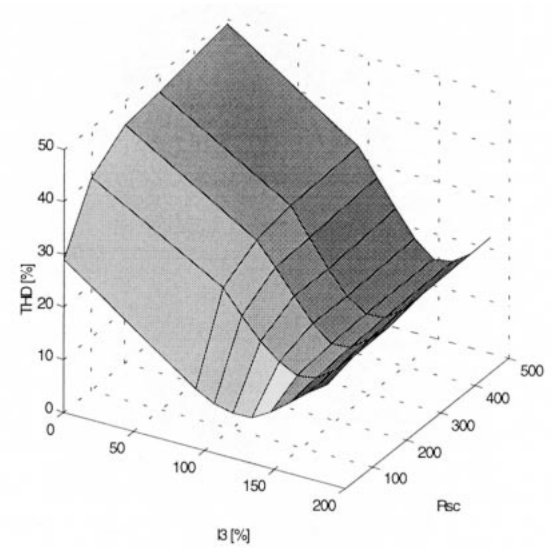

Fig. 4. Current THD of the input power as a function of the circulating current in percentage of the output current and the short-circuit power. The dc-link inductance of the six-pulse diode rectifier equals 2.6%.

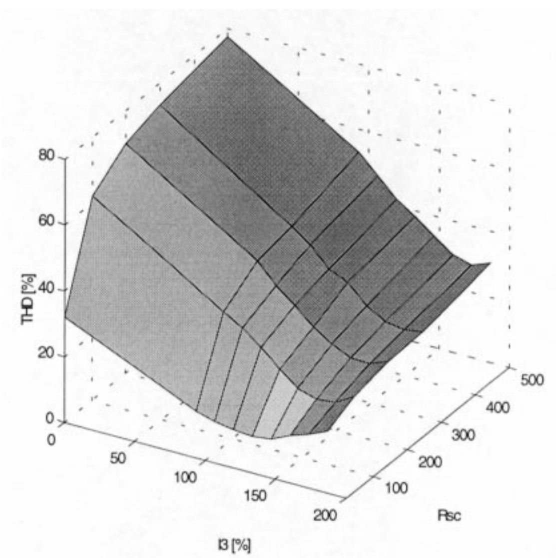

Fig. 5. Current THD of the input power as a function of the circulating current in percentage of the output current and the short-circuit power. There is no dc-link inductance in the six-pulse diode rectifier.

It can be seen from Fig. 4 that using a dc-link inductance of 2.6% and a circulating current (I_3) of approximately 150% of the output current (I_o) results in an input current THD of less than 15% and it is independent of the line reactance. On a weak utility grid ($R_{sc} = 20$), a circulating current of 120% gives a minimum THD of 9%. Fig. 5 shows that the circulating current has to be somewhat higher (180%) when no dc-link inductance is used. Only at a weak grid ($R_{sc} = 20$) can an input current THD of 15% be achieved. Here, the circulating current (I_3) has only to be 140% of the output current (I_o).

The power dissipated in the resistor equals the circulating current times the voltage V_{hN}. The voltage V_{hN} and the current I_3 can be presented as [8]

$$V_{hN} = V_{ab}\,\frac{-3\sqrt{2}}{8\pi}\,\sin(3\omega t)$$
$$I_3 = -\hat{I}_3\,\sin(3\omega t) \tag{4}$$

where ω is the angular frequency of the fundamental voltage of utility grid.

The instantaneous power losses in the resistor R_e can be calculated as

$$P_{3,\text{inst}} = V_{ab}\hat{I}_3\,\frac{3\sqrt{2}}{16\pi}\,(1-\cos(6\omega t)). \tag{5}$$

It should be noted that, by employing the boost converter to emulate the variable resistor R_e (Fig. 2), the only power losses are the switching and conduction losses in the converter.

IV. Performance of the Proposed Scheme

For galvanic isolation of the boost converter, a single-phase transformer is required. The output of the boost converter is connected to the dc-link capacitor bank of the ASD and, therefore, the boost converter needs no outer voltage loop control. For integration of the boost converter in the ASD, the diode and the IGBT of the braking chopper circuit of the standard ASD is used.

To evaluate the proposed scheme, some simulations are made using the SABER simulator. The simulated system consists of a 10-kW three-phase rectifier, 480-V line-to-line voltage, and the frequency is 60 Hz. The utility grid is modeled by some line inductance. The base impedance of the rectifier equals $Z_b = 23.04\ \Omega$ (calculated as defined in Section II). The total capacitance of the dc-link capacitor banks equals 10.5% of the base impedance. The transformers are ideal with no leakage inductance and a high magnetizing inductance. The transformer ratio of the single-phase transformer is 1:4. The switching frequency of the boost converter is about 8 kHz. The short-circuit ratio R_{sc} is varied from 20 to 500. Again, simulations are made with and without a 2.6% dc-link inductance.

A. With DC-Link Inductance

As expected, varying the ac-line impedance and thereby the short-circuit ratio has shown that there is small difference in the behavior of the proposed system between a weak and a strong utility grid. The current and the Fourier spectrum of the current are shown in Figs. 6 and 7.

The THD of the current is 9% with a short-circuit ratio of 20, while the THD is 13% with a short-circuit ratio of 500. The amplitude of the circulating current on the primary side of the single-phase transformer is 17.7 A (rms). The output current I_o equals 15 A.

B. Without DC-Link Inductance

As expected, without the dc-link inductance the harmonic distortion of the input current is increased at a high short-circuit ratio. This is shown in Fig. 8. The THD of the current is 23.6%,

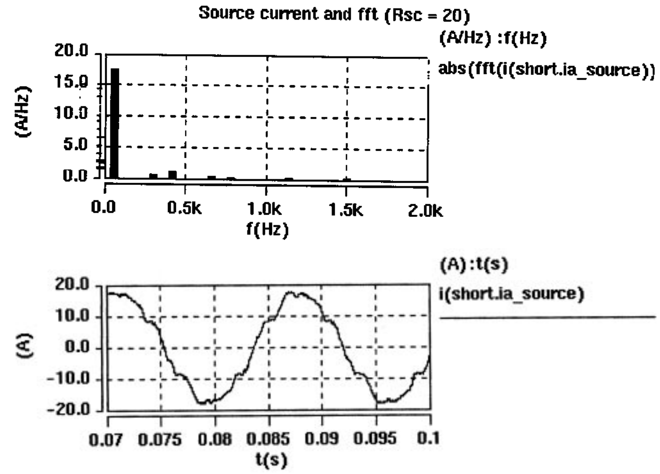

Fig. 6. Line current and the Fourier spectrum. The short-circuit ratio $R_{\text{sc}} = 20$ and the THD of the line current is 9%.

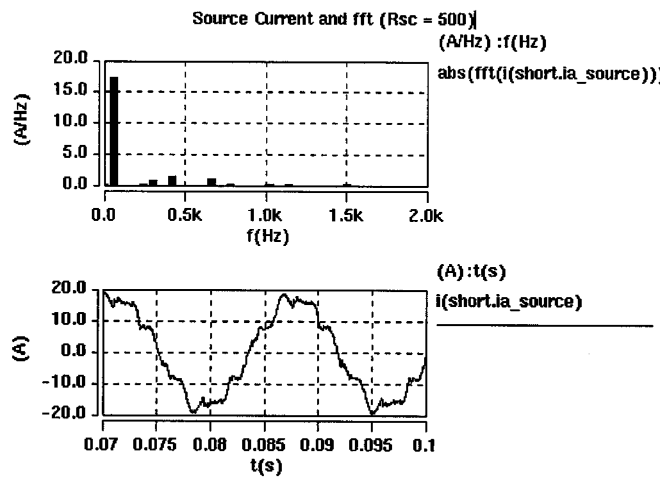

Fig. 7. Line current and the Fourier spectrum. The short-circuit ratio $R_{\text{sc}} = 500$ and the THD of the line current is 13%.

while the short-circuit ratio equals 500. The amplitude of the circulating current on the primary side of the single-phase transformer is 21.1 A (rms). The output current I_o equals 15 A.

In a system with a weak utility grid, the performance of the proposed solution is almost as good as with the dc-link inductance. This is shown in Fig. 9. The THD of the current is 10% with a short-circuit ratio of 20. The amplitude of the circulating current on the primary side of the single-phase transformer is the same as that with dc-link inductance, 17.7 A (rms). The output current I_o equals 15 A.

C. Adaptation of the Proposed Scheme for Multiple Drives

Interconnection of multiple drives is also possible. Two 10-kW ASD's are connected in parallel as shown in Fig. 10. By interconnection of the dc link, it is assured that both diode rectifiers are equally loaded, even when one of the ASD's is braking. For preventing load oscillations, the connection has to be made on the line side of the dc-link inductance. The midpoints of the dc-link capacitors in the ASD's are connected

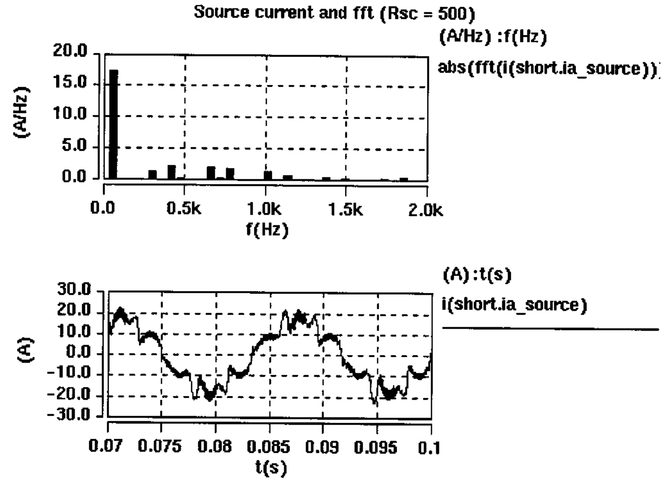

Fig. 8. Line current and the Fourier spectrum. The short-circuit ratio $R_{\rm sc} = 500$ and the THD of the line current is 23.6%.

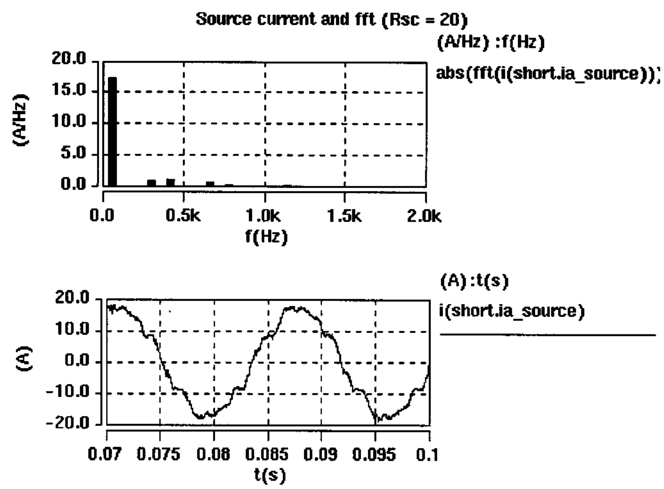

Fig. 9. Lline current and the Fourier spectrum. The short-circuit ratio $R_{\rm sc} = 20$ and the THD of the line current is 10%.

together to ensure that the circulating current is divided equally between both rectifiers.

Fig. 11 shows the result when both drives are operating under full-load condition. The simulations are made with a short-circuit ratio $R_{\rm sc} = 100$. Fig. 12 shows the result when one of the drives operates at half load and the other drive operates at full load. It is shown that the differences in the loads of both drives do not influence the harmonic performance of the proposed scheme. The current THD equals 11.6% and 12.5%, respectively.

D. Discussion of the Simulated Results

It is demonstrated that, for a low short-circuit ratio, a single-digit current THD can be achieved, and when series inductance (either dc or ac inductance) is used, as in the case with the dc-link inductance, a THD well below 15% can be achieved, even for a (very) high short-circuit ratio. Only in the case of no series inductance and a high short-circuit ratio is the result not satisfying. Also, the circulating current becomes somewhat

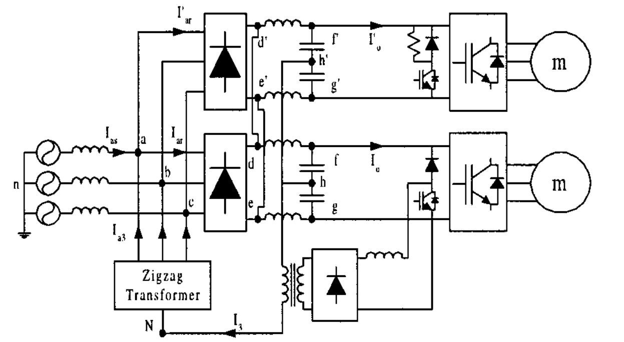

Fig. 10. Interconnection of two ASD's. One uses the dynamic braking chopper for the proposed scheme, while the other uses the dynamic braking chopper for braking resistor.

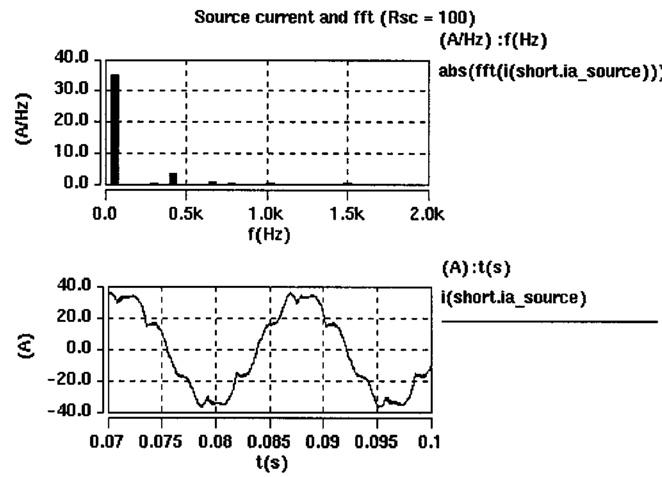

Fig. 11. Line current and the Fourier spectrum with interconnection of two ASD's. The THD of the line current is 11.6%. Both ASD's operate at full load.

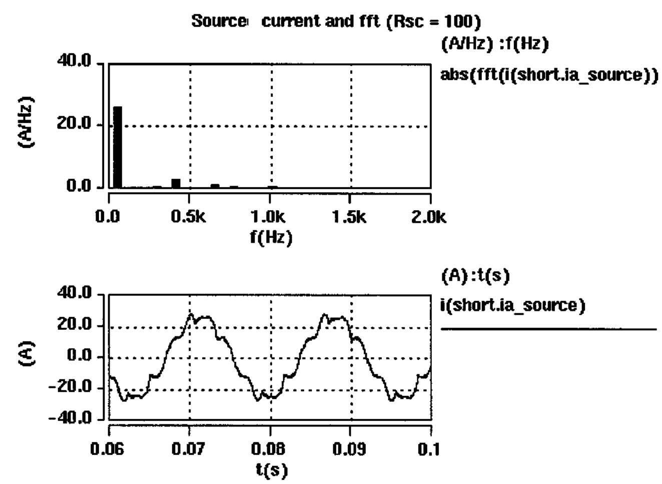

Fig. 12. Line current and the Fourier spectrum with interconnection of two ASD's. The THD of the line current is 12.5%. One ASD operates at full load while the other operates at half load.

higher in this case. To fulfill the demands of independent operation of the line impedance, stated in Section I, one should use an additional inductance. Either an ac inductance or, as presented in this paper, a split dc-link inductance can be used. However,

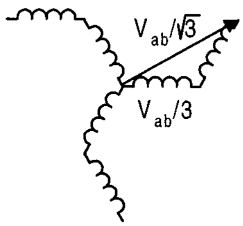

Fig. 13. Voltage across the windings on a zigzag transformer.

the interconnection of multiple drives should only be done when dc-link inductances are used to prevent load oscillations.

V. Design Example

In this section, the design of the zigzag transformer, the single-phase transformer, and the boost converter are presented in per-unit quantities.

Ratings of various components are calculated based on a rectifier using a dc-link inductance, hence, $I_3 = 1.20 * I_o$.

A. Zigzag Transformer Voltampere Rating

The voltage across the zigzag transformer is illustrated in Fig. 13. The voltage on the primary (and secondary) winding V_{wd} of the transformer is

$$V_{wd} = \frac{V_{an}}{\sqrt{3}} = \frac{V_{ab}}{3}. \qquad (6)$$

The current in the phase windings (I_{a3}) is $1.2 * I_o/3$. Thus, the voltampere rating of the transformer is

$$VA_{\text{zigzag}} = 3\,\frac{V_{ab}}{3}\,\frac{1.2 \cdot I_o}{3} = \frac{1.2 \cdot I_o \cdot V_{ab}}{3} = 0.296 \text{ pu}. \qquad (7)$$

B. Single-Phase Transformer and Boost Converter Voltampere Rating

The transformer ratio of the single-phase transformer should be chosen with care. Since no outer voltage control loop is necessary, the output of the boost rectifier is connected directly to the capacitor banks of the ASD. In a boost converter, the dc-link voltage must always be somewhat higher than the amplitude of the input voltage. In [8], it is shown that V_{hN} basically is given by $V_{hN} = 0.169 V_{ab}$. Since the output voltage is $1.35 V_{ab}$ and a boost factor of 1.5 is normal for a boost converter, the transformer ratio "k" can be calculated as

$$k = \frac{1.35 \cdot V_{ab}}{1.5 \cdot 0.169 \cdot \sqrt{2} \cdot V_{ab}} = 3.77. \qquad (8)$$

The voltampere rating of the single-phase transformer is then given by

$$VA_{\text{single-phase}} = 0.169 \cdot V_{ab} \cdot 1.2 \cdot I_o = 0.15 \text{ pu}. \qquad (9)$$

The single-phase transformer has to be designed to operate at a frequency of three times the fundamental line frequency. The voltampere rating of the boost converter is the same as the voltampere rating of the single-phase transformer.

VI. Experimental Results

An experimental setup is built in the Power Quality and Power Electronics Laboratory, Texas A&M University, College Station. The rectifier of a 480-V 10-kW commercial ASD is used to be retrofitted with the proposed approach.

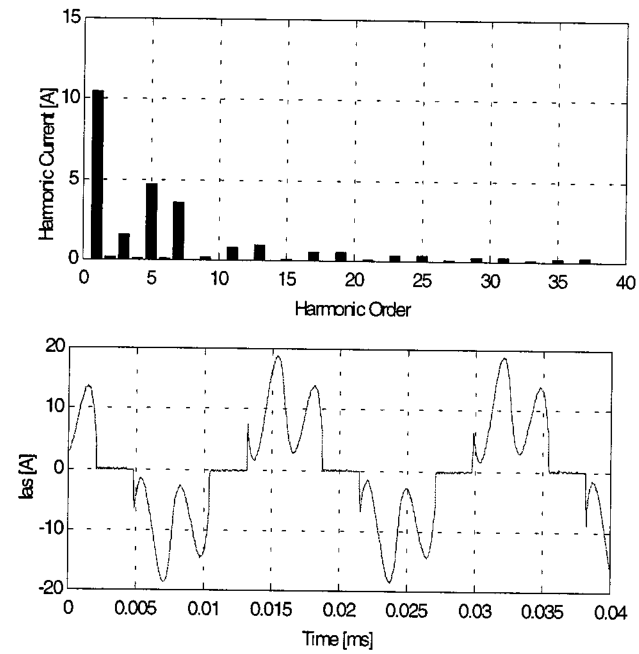

Fig. 14. Fourier spectrum and a time plot of the line current without use of the proposed scheme. Current THD = 60%. Load is approximately 5.8 kW.

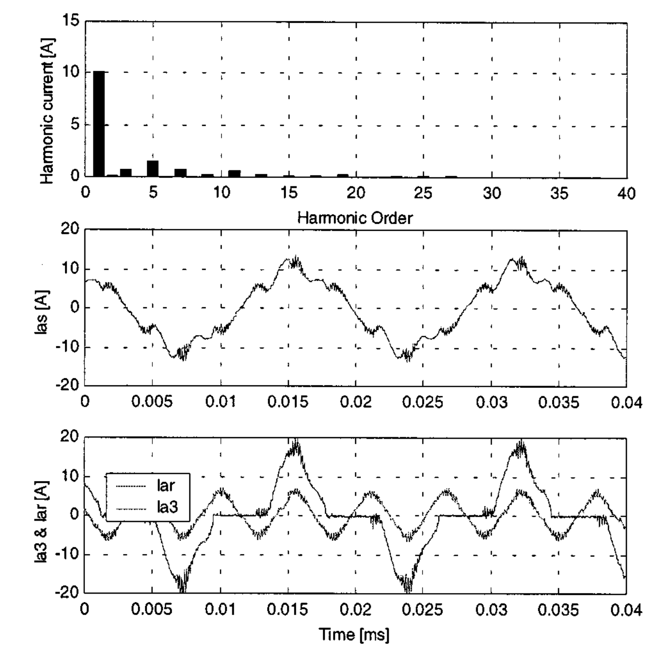

Fig. 15. Fourier spectrum and a time plot of the line current with the use of the proposed scheme. Current THD = 19%. Load is approximately 5.8 kW. Lower plot shows the third harmonic current of one transformer phase as well as the phase current in the diode rectifier itself.

The value of the dc-link inductance is 1.6 mH (2.6%) and the value of the two dc-link capacitors is 2.2 mF (total 10.5%). The rectifier is connected close to a 480-V 60-Hz 75-kVA transformer with 6% short-circuit impedance. Therefore, the short-circuit ratio is approximately 125. The rectifier is loaded with a 77-Ω power resistor; this equals approximately 5.5 kW.

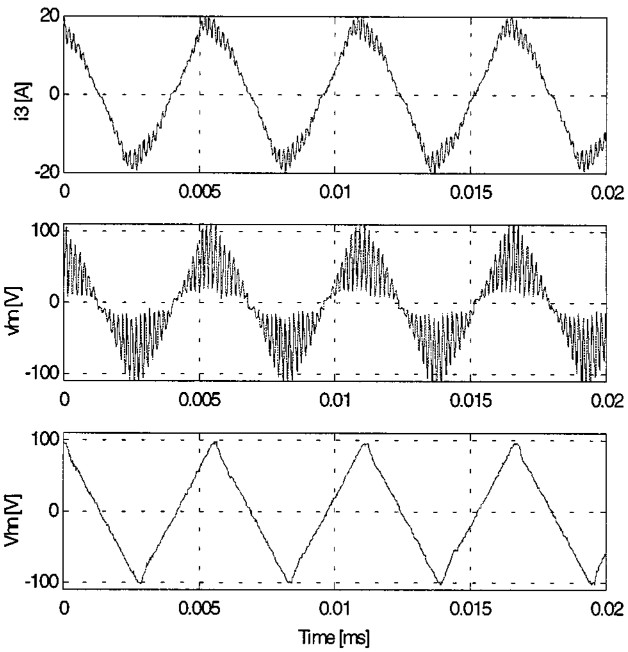

Fig. 16. Current and voltage of the primary side of the single-phase transformer. Lower plot shows the voltage V_{hN} when the converter is not switching.

The boost converter is of the continues conduction mode (CCM) type. The control is performed by two integrated circuits (current controller and multiplier). The reference to the current controller is given by multiplying the rectified voltage V_{hN} and an rms current reference. The rms current reference is in this setup given manually. The switching frequency is about 6 kHz.

Fig. 14 shows the line current and the Fourier spectrum without the proposed approach. The power is about 5.8 kW. The current THD equals 60%. Also, a small amount of a third harmonic current can be seen, which indicates some degree of unbalance on the utility grid.

Fig. 15 shows the line current and the Fourier spectrum with the proposed approach. The current THD equals 19%. It is clearly shown that the amount of the fifth and seventh harmonic current is significantly reduced. The lower plot of Fig. 15 shows the phase current of the zigzag transformer I_{a3} and the current of the rectifier I_{ar}. It should be noted that the peak current of the rectifier is not higher with the new proposed approach than without, so no derating of the diodes is necessary.

Fig. 16 shows the current and the voltage on the primary side of the single-phase transformer V_{hN}. The lower plot of Fig. 16 shows the voltage while the converter is not switching. It can be seen that the current I_3 is in shape and phase with the voltage V_{hN}.

VII. Conclusion

In this paper, an integrated single-switch approach to improve harmonic performance of standard PWM-ASD's has been presented. The approach is essentially an add-on solution to standard ASD's. The proposed scheme has shown that significant reduction of ASD-generated harmonics is possible with the proposed approach. The advantages compared to other solutions, such as no extra components (extra losses) in series with the power flow and independence of the line impedance, makes this approach a potential solution for ASD's.

Also, advanced programming of the current reference has not been considered so far, but it is likely that applying a more intelligent current control than used in this paper can reduce the harmonic current distortion further. Future work on this scheme should, therefore, consider this possibility.

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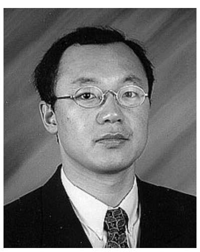
Steffan Hansen (S'95–A'96–M'99) was born in Sonderburg, Denmark, in 1971. He received the M.Sc.E.E. degree in 1996 from Aalborg University, Aalborg East, Denmark, where he is currently working toward the Ph.D. degree through an industrial fellowship supported by Danfoss Drives A/S and the Danish Academy of Technical Sciences.

Since 1996, he has been with Danfoss Drives A/S, Graasten, Denmark. His research interests are the control of active rectifiers and active filters, harmonic current and voltage distortion of diode rectifiers, power converter topologies for improved harmonic performance, and sensorless control of induction and switched reluctance motors.

Prasad N. Enjeti (S'86–M'88–SM'95–F'00) received the B.E. degree from Osmania University, Hyderabad, India, the M.Tech degree from the Indian Institute of Technology, Kanpur, India, and the Ph.D. degree from Concordia University, Montreal, PQ, Canada, in 1980, 1982, and 1988, respectively, all in electrical engineering.

In 1988, he joined the Department of Electrical Engineering Department, Texas A&M University, College Station, as an Assistant Professor. In 1994, he became an Associate Professor and, in 1998, he became a Professor. His primary research interests are advance converters for power supplies and motor drives, power quality issues and active power filter development, and utility interface issues and "clean power" converter designs. He is the holder of two U.S. patents and has licensed two new technologies to industry. He is the Lead Developer of the Power Quality Laboratory at Texas A&M University and is actively involved in many projects with industry while engaged in teaching, research, and consulting in the areas of power electronics, motor drives, power quality, and clean power utility interface issues.

Dr. Enjeti was the recipient of numerous IEEE Industry Applications Society (IAS) Best Paper Aawards, the Second Best Paper Award published in mid-year 1994 to mid-year 1995 from the IEEE TRANSACTIONS ON INDUSTRY APPLICATIONS, and the *IEEE Industry Applications Magazine* Prize Article Award in 1996. He is a member of the IAS Executive Board and the Chair of the Standing Committee on Electronic Communications. He is a Registered Professional Engineer in the State of Texas.



Jae-Hong Hahn (S'98) received the B.S. degree from Seoul National University, Seoul, Korea, in 1989. He is currently working toward the Ph.D. degree in power electronics at Texas A&M University, College Station.

From 1989 to 1994, he was a Design Engineer in the Research and Development Center, Daewoo Heavy Industries, Incheon, Korea. From 1994 to 1995, he was a Field Application Engineer with Linear Technology Corporation. From 1995 to 1996, he was with Maxim Integrated Products Inc. as a Senior Field Application Engineer. His interests are in power electronics applications to power quality and clean power converters.

Frede Blaabjerg (S'86–M'88–SM'97) was born in Erslev, Denmark, in 1963. He received the M.Sc.E.E. degree from Aalborg University, Aalborg East, Denmark, and the Ph.D. degree from the Institute of Energy Technology, Aalborg University, in 1987 and 1995, respectively.

He was with ABB-Scandia, Randers, Denmark, from 1987 to 1988. He became an Assistant Professor at Aalborg University in 1992. In 1996, he became an Associate Professor and, in 1998, he became a Professor of power electronics and drives. His research interests include power electronics, static power converters, ac drives, switched reluctance drives, modeling, characterization of power semiconductor devices, and simulation. He is currently involved in several research projects with industry. Among them is the Danfoss Professor Programme in Power Electronics and Drives.

Dr. Blaabjerg is a member of the European Power Electronics and Drives Association and the Industrial Drives, Industrial Power Converter, and Power Electronics Devices and Components Committees of the IEEE Industry Applications Society (IAS). He is the Paper Review Chairman of the Industrial Power Converter Committee of the IAS. He is a member of the Danish Technical Research Council and a Member of the Board of the Danish Space Research Institute. He received the 1995 Angelos Award for his contributions to modulation technique and control of electric drives, and the 1995 Annual Teacher Prize from Aalborg University. In 1998, he received the Outstanding Young Power Electronics Engineer Award from the IEEE Power Electronics Society and the IEEE TRANSACTIONS ON POWER ELECTRONICS Prize Paper Award for best paper published in 1997. He also received two Prize Paper Awards at the IAS Annual Meeting in 1998.