

A New Space-Vector-Based Control Method for UPS Systems Powering Nonlinear and Unbalanced Loads

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Abstract—In this paper, a new real-time space-vector-based control strategy is presented for three-phase uninterruptible power supply systems powering nonlinear and unbalanced loads. The proposed control strategy generates the inverter reference and gating signals in closed loop and guarantees high-quality output voltages at the load terminals. The approach, which is implemented on a digital signal processor, adapts to a wide variation of nonlinear and unbalanced load conditions without specific knowledge of the output filter (L - C) component values. Analysis and experimental results on a 10-kVA prototype are presented. The results show that the output voltage is restored at heavy nonlinear and unbalanced load.

Index Terms—Control, ground power units, modulation, power converters, unbalanced load, uninterruptible power supply.

I. INTRODUCTION

WITH THE RAPID growth in the utilization of rectifiers for critical loads, e.g., in computers or in medical equipment, the need for high-quality uninterruptible power is increasing. Nonlinear currents drawn by rectifier loads distort the output voltage of uninterruptible power supply (UPS) systems mainly because of the output filter impedance in the UPS. A distorted output voltage will result in a reduced dc-bus voltage of rectifier loads and may lead to excessive losses and heating.

The output filter in the UPS is necessary due to the distorted pulsewidth-modulated (PWM) waveform generated by the inverter. In low-power supplies, the switching frequency of the inverter may be increased in order to reduce the need for filtering. However, at higher power levels, the switching frequency is limited by the switching devices.

The PWM inverter in a UPS is typically filtered with an LC filter, where the L element is up to 0.05 pu (60-Hz systems) or 0.3 pu (400-Hz systems) in order to reduce the amplitude of the switching currents [1]. Currents of higher frequencies drawn through this element will cause heavy distortion on the output.

Nonlinearities of the inverter system, e.g., blanking time, rise/fall times of the devices, switching delays, fluctuating

dc-bus voltage, and component voltage drop generate lower order harmonics on the output [6]. In order to achieve a high-quality output, both the load and the inverter-induced harmonics and unbalance have to be compensated to a minimum. Different approaches have been taken in order to reduce the voltage distortion in such systems.

In [7], a deadbeat controller with voltage and current feedback is applied. The control scheme uses the state feedback information to compensate for the inductor voltage drop. This scheme is very dependent on precise knowledge of the filter components and requires measuring of both filter current, load current, and output voltage. The scheme also includes prediction algorithms to compensate for the controller and system delays. Unfortunately, the scheme will not compensate for the inverter-induced harmonics.

In [2] and [9] selected harmonics on the output are identified by a discrete Fourier transformation (DFT). The mean values of selected harmonics of the three phases are used as feedback to an integrating controller, which is applied to the control signal of the inverter. In this way, selected balanced harmonics can be removed. Unfortunately, unbalanced distortion cannot be removed by this method.

In [3], a repetitive learning controller is used instead to adapt the switching function to compensate for the harmonics. This scheme requires also very good information about the filter components in order to apply the inverse filter transfer function.

This paper presents a new real-time digital compensator implemented in a digital-signal-processor (DSP)-based system that adapts to both nonlinear and unbalanced load without exact knowledge of the output-filter components. The compensation is based on the vectorial voltage error on the output. The control principle can also be used in other static power converters like ac power supplies and 400-Hz ground power units [11]. The performance is verified on a 10-kVA test system.

II. SYSTEM DESCRIPTION

A typical UPS system has a power circuit as shown in Fig. 1. The utility power is rectified and filtered by an input choke and the dc capacitor. A battery pack is normally connected to the dc link to supply power during utility outage. The output voltages are generated by an insulated-gate-bipolar-transistor (IGBT)-based pulsewidth-modulated (PWM) inverter. The switching ripple is filtered by an LC filter. The output transformer provides galvanic isolation and generates the neutral by a delta-star connection. By keeping the inductive part of the filter on the primary side of the transformer, zero-sequence

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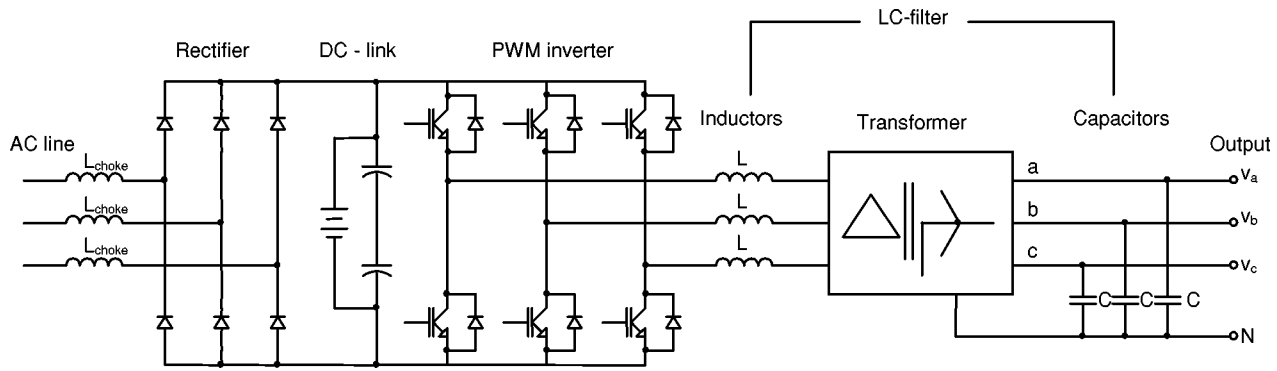


Fig. 1. Circuit of a typical PWM-based three-phase UPS system.

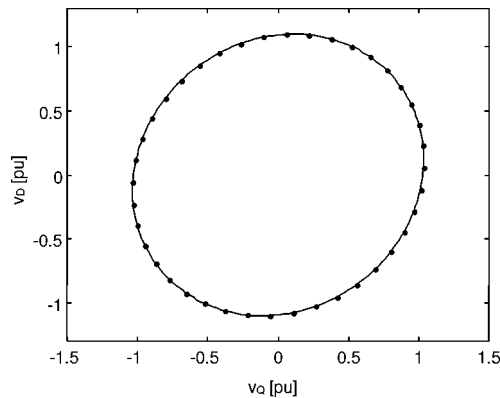


Fig. 2. Output voltage vector locus at unbalanced load. The PWM inverter generates sinusoidal voltages.

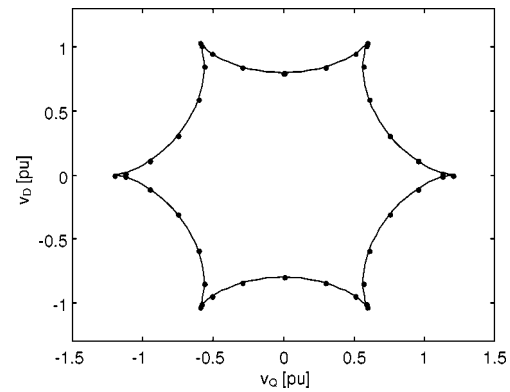


Fig. 3. Output voltage vector locus at nonlinear load. The PWM inverter generates sinusoidal voltages.

currents on the output will be shorted in the delta winding by a strong transformer coupling.

The output voltages are sensitive to the load current at non-linear load, where current components of higher frequencies are present. Close to the resonance frequency of the *LC* filter, the output impedance of the filter is very high. In Figs. 2 and 3, the output voltage vector locus is shown for two different load situations where the inverter is driven with a circular reference voltage vector locus, when the three phases are transformed into a two-axes representation by (1). Figs. 2 and 3 illustrate the relationship between nonlinear and unbalanced loads and output voltage distortion. In Fig. 2, the load is unbalanced, with linear load in two phases and no load in the third phase. The output voltage vector becomes oval. In Fig. 3 the UPS system is loaded with a three-phase rectifier load. The output voltage is distorted into an almost hexagon form due to the fifth and seventh harmonic load currents. (In the vectorial plane, they are both shown as a sixth harmonic due to their respective negative and positive rotational direction compared to the fundamental.) In the cases shown in Figs. 2 and 3, the voltages are sampled 40 times per fundamental period. In both cases, both amplitude and angular errors exist when compared to a regular sampled circle.

To control the inverter in a way that compensates for both amplitude and angular errors compared to a circular voltage vector locus, a vectorial approach has to be taken. In order to fix the control system to the fundamental frequency, the inverter will be driven with a synchronous modulation function. In that way,

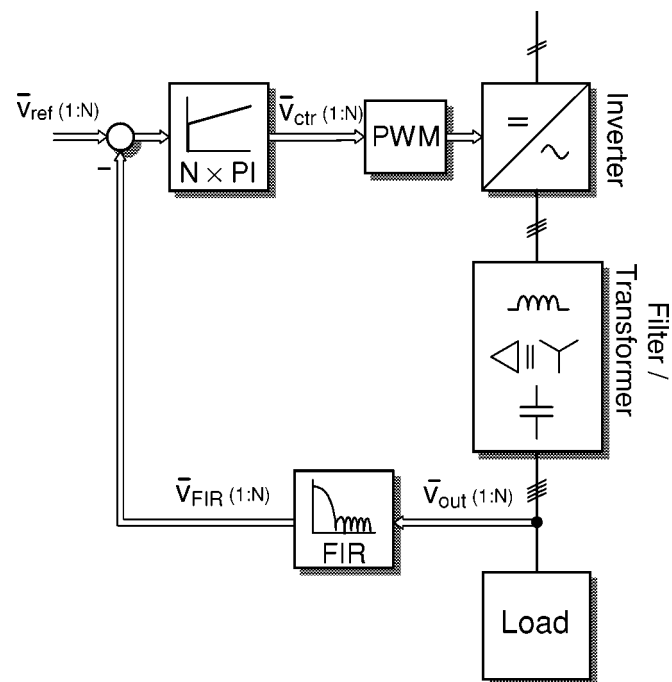


Fig. 4. Proposed concept of the control system for a high-performance UPS.

the individual switching periods will have a fixed relation to the fundamental period and it gives the possibility for introducing a repetitive control strategy.

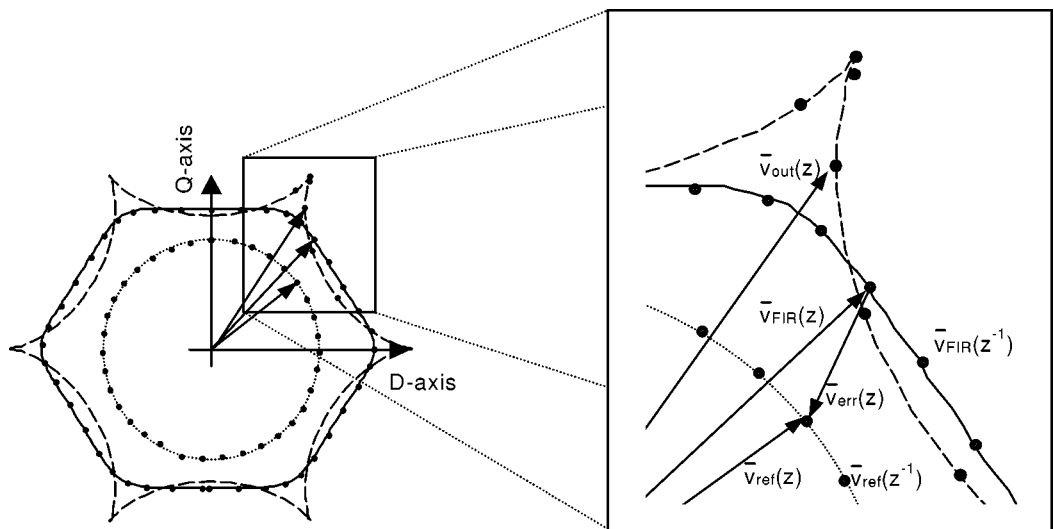


Fig. 5. Illustration of the variables in the control system: reference voltage vector (.), output voltage vector (—), and filtered output (---), when a strong nonlinear load is just applied.

TABLE I
CONTROLLER PARAMETERS FOR PI CONTROL

	Proportional gain	Integration Time
Ziegler-Nichols	0.45·K _u	T _u /1.2
Damping ~ 1.0	0.4·K _u	T _u /1.2

TABLE II
TEST SETUP PARAMETERS

Nominal output voltage	U _{nom}	3x115/200 V
Output filter inductor	L	410 μH
Output filter capacitor	C	30 μF
Transformer ratio	N _{transformer}	0.4
Fundamental frequency	f _{fund}	60 Hz
Switching frequency	f _{switch}	6 kHz
Samples per fundamental period	N	200
Output filter resonance frequency	f _{resLC}	2.0 kHz

III. PROPOSED CONTROL STRATEGY

This section describes the algorithms of the proposed control strategy. The output voltages of the system are sampled and converted into a vector representation by the Park transformation (1)

$$\bar{v}_{out} = \begin{bmatrix} v_D \\ v_Q \end{bmatrix} = \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & -\frac{\sqrt{3}}{2} & \frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} \quad (1)$$

where \bar{v}_{out} is the output voltage vector, $v_{a..c}$ are the three line-to-neutral output voltages, and $v_{D,Q}$ are the output voltages transformed into vectorial components.

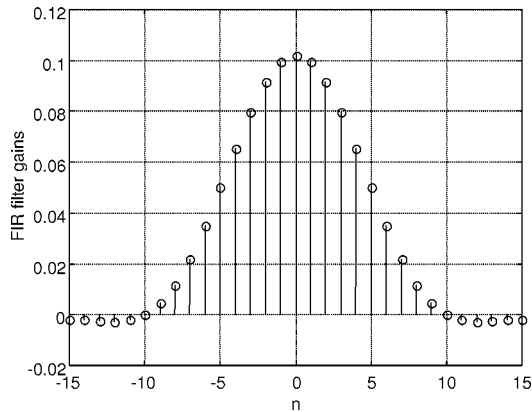


Fig. 6. Impulse response/filter gains of zero-phase lag FIR filter, used for the feedback signal in the control loop.

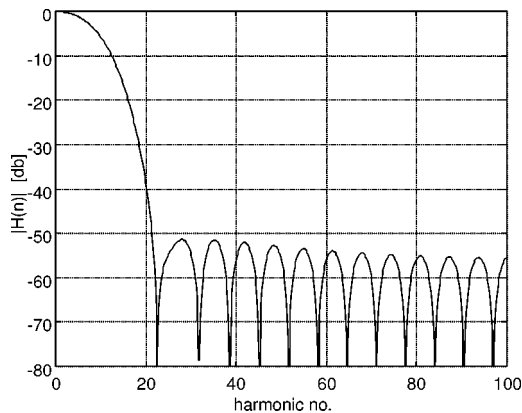


Fig. 7. Amplitude characteristics of FIR filter, used for the feedback signal in the control loop.

This transformation converts symmetrical nondistorted output voltages into a perfect circle. With the vector representation, all positive- and negative-sequence components of a three-phase system can be represented as a deviation from the perfect circle. The zero-sequence components are neglected by

TABLE III
 LOAD PARAMETERS

L_{cable}	10.1 μ H
R_{cable}	0.1 Ω
C_{DC}	6000 μ F
R_{DC}	2.0 Ω

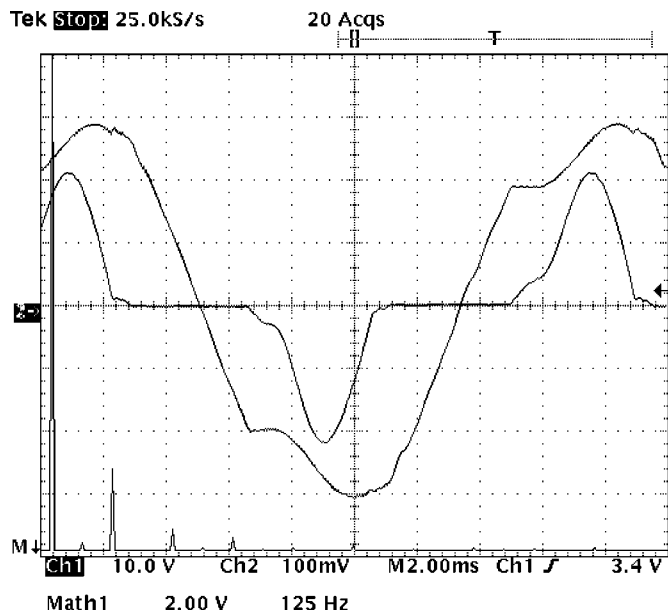


Fig. 8. Measured output voltage, harmonic contents, and output current (10 A/100 mV) without compensation at single-phase nonlinear load.

the transformation. With the applied inverter topology, zero-sequence components cannot be controlled, so the transformation does not reduce the controllability of the whole system. The controller output voltages and reference voltages can also be represented by voltage vectors by the transformation in (1).

In order to achieve a circular output voltage vector at all loads, the inverter voltages have to be controlled in a way that compensates for the load and inverter-induced harmonics of lower order. The higher order harmonics are damped by the output filter.

By introducing N different inverter references, one per sample per fundamental period, the single inverter references can be controlled and updated once per fundamental period. The individual errors of N points of one fundamental period are the deviation of the output voltage to the reference in each point.

With a pure integrating controller structure the control equation is then given by

$$\bar{v}_{ctr}(z) = \bar{v}_{ctr}(z - N) + K \cdot (\bar{v}_{ref}(z) - \bar{v}_{FIR}(z)) \quad (2)$$

where K is the controller gain, z indicates the present circular position of the voltage vector, \bar{v}_{ctr} is the controller output vector, \bar{v}_{ref} is the reference vector, \bar{v}_{FIR} is the filtered feedback, and N is the number of samples per fundamental period.

This type of controller is referred to as a ‘‘repetitive controller’’ as discussed in [3] and [10]. This structure can also be extended to a proportional plus integral (PI) controller structure

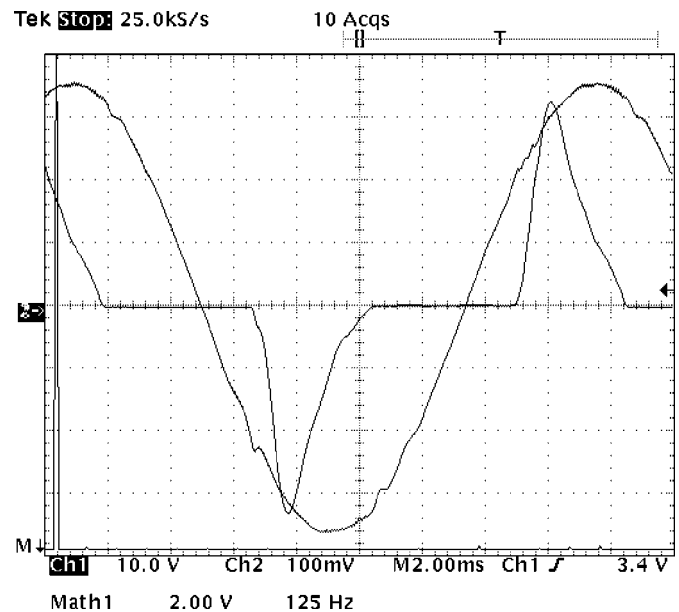


Fig. 9. Measured output voltage, harmonic contents, and output current (10 A/div) with compensation at single-phase nonlinear load.

 TABLE IV
 VOLTAGE AND CURRENT DISTORTION

	Voltage THD%	Current THD%
Without correction	14.0	76
With correction	1.54	89

in order to improve stability and obtain a faster response. With a PI controller structure, the control equations are given by

$$\begin{aligned} \bar{v}_{err}(z) &= \bar{v}_{ref}(z) - \bar{v}_{FIR}(z) \\ \bar{v}_{ctr}(z) &= \bar{v}_{ctr}(z - N) + K \cdot \bar{v}_{err}(z) - K \cdot (1 - T_s/T_i) \\ &\quad \cdot \bar{v}_{err}(z - N) \end{aligned} \quad (3)$$

where \bar{v}_{err} is the error between reference and filtered output, T_s is the sampling time, and T_i is the integration time of the controller.

With an integrating structure, the controller will be sensitive to the phase lag of the LC filter. At frequencies above the LC filter resonance frequency, the phase lag of the LC filter approaches 180° asymptotically. The frequency content in the output voltage must be filtered in the control system only to contain frequencies with a phase lag below 135° in order to ensure stability in the control loops [8]. In order not to introduce any additional phase lag, a digital zero-phase-shift low-pass finite-impulse response (FIR) filter is introduced. The filter is noncausal, but due to the fundamental periodicity of the system, the filter can be applied by using some samples from the previous fundamental period. The proposed controller concept is shown in Fig. 4.

The principle of the control process is visualized in Fig. 5. The output voltage vector \bar{v}_{out} is heavily distorted by a nonlinear load. Before entering the integrating controller, the output

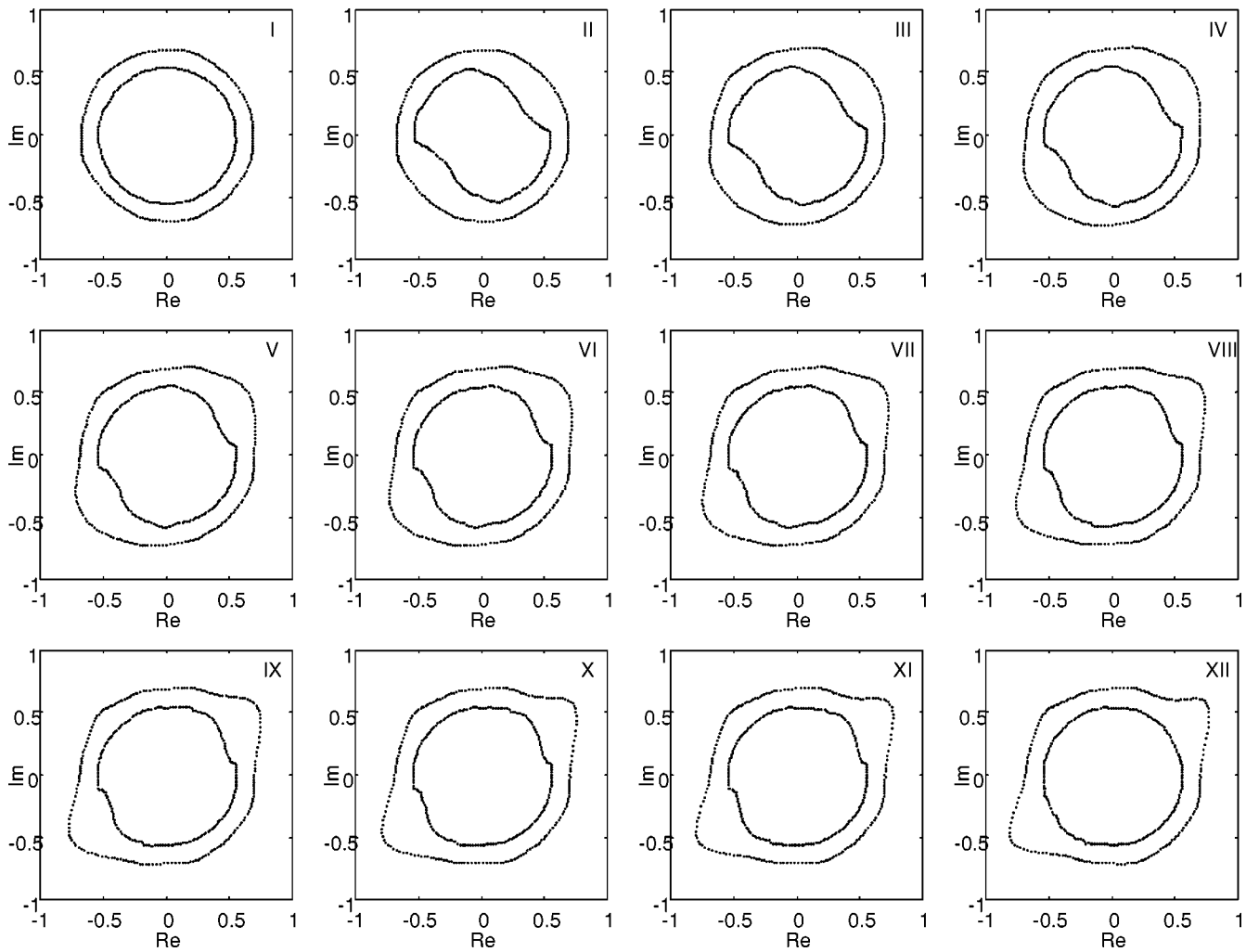


Fig. 10. Measured output voltage vector v_{out} (inner) and reference voltage vector v_{ref} (outer) loci at different stages of the adaptation at an unbalanced and nonlinear load. Phase I: no load; phase II: heavy load introduced; phases III–IX: adaptation to the load; phase XII: compensated output voltage.

is filtered by the zero-phase-lag FIR filter (corner frequency of FIR filter is decreased for illustration). The filtered output vector contains only lower frequency errors both in amplitude and phase. The error between the filtered output voltage and the reference is input to the controller. In the next sample, this process is repeated. The output voltage vector values and the controller output vector values are periodically stored in arrays in order to be used in the next fundamental period.

IV. DESIGN OF CONTROL PARAMETERS

The controller in (3) is for each of the N positions updated only once per fundamental period. The dynamics of the system and the controller is dominated by this large delay. Compared to the dynamic of the filter alone, the delay of one fundamental period will be several times slower.

By assuming that the dynamics in the system are determined by the delay alone, the PI-controller can be designed by a method used for auto-tuning, the relay experiment [8]. With the system in a limit cycle oscillation caused by the relay, the ultimate period time T_u can be approximately determined as the frequency of the limit cycle, where the system has a phase

lag of 180° . The ratio between the amplitude of the limit cycle and the relay amplitude is approximately the process gain at that frequency K_u . From that Ziegler–Nichols ultimate period method can be used to find suitable values for the controller parameters as specified in Table I.

With a delay of one fundamental period, the system will have a limit cycle frequency of one fundamental period. Therefore, T_u is equal to $1/60$ s. The settle time will be approximately ten fundamental periods, when the controller is designed to settle with a damping factor of 1.0 and updated once per fundamental period. The system gain at 60 Hz is approximately the inverter gain multiplied by the transformer ratio $N_{transformer}$.

As explained above, the control parameters are dependent more on the delay of the control system than on the filter parameters. This eases the implementation with different filter configurations. Only the FIR filter has to cut off lower than the LC filter resonance to ensure stability in the control loops.

V. IMPLEMENTATION

The proposed control strategy has been implemented on a 10-kVA prototype with specifications as shown in Table II.

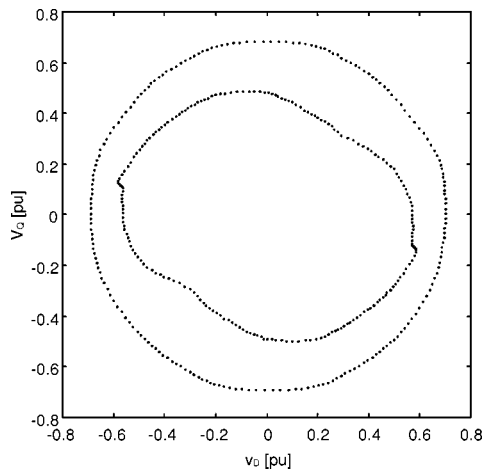


Fig. 11. Measured output voltage vector $v_{o, out}$ (inner) and reference voltage vector v_{ref} (outer) without compensation at unbalanced load.

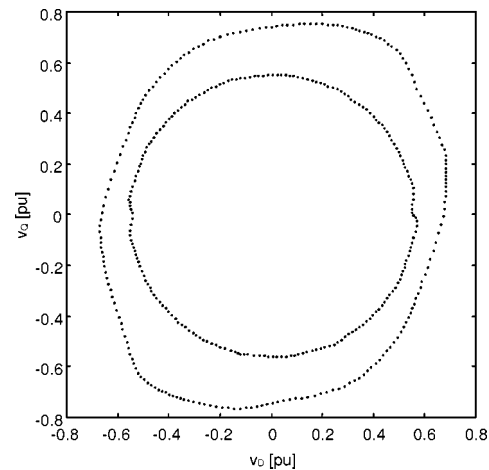


Fig. 12. Measured output voltage vector $v_{o, out}$ (inner) and reference voltage vector v_{ref} (outer) with compensation at unbalanced load.

An Analog Devices 21062 DSP extended with A/D conversion and pulse generation circuits controls the system. The control system can be operated from a PC. One fundamental period is divided into 200 samples (same as the synchronous modulation scheme applied), resulting in a sample time of $83.3 \mu\text{s}$.

Implementing the FIR filter, the selectivity (damping slope) depends on the filter order. In the following tests, a 30th-order FIR filter has been used. The FIR-filter characteristics are shown in Figs. 6 and 7. The coefficients have been calculated by using a Hamming window function. This improves the damping level above the cutoff frequency [12].

VI. EXPERIMENTAL RESULTS

The proposed control strategy has been tested on different nonlinear and unbalanced loads. In the following experiment, a single-phase diode rectifier has been connected between output phase a and the neutral through a small inductance. The rectifier has a large dc capacitor C_{DC} with a resistive load R_{DC} . The parameters of the load setup are shown in Table III.

Without any compensation and with constant inverter reference, the output voltage and the output current of phase a are shown in Fig. 8 with heavy distortion of the output voltage. With the new control strategy applied, the harmonic voltage drop is compensated and the distortion is considerable lower as seen in Fig. 9. The voltage and current distortions before and after the compensation are shown in Table IV.

In Fig. 10, the compensation of the nonlinear and unbalanced load is shown. In part I of Fig. 10, the system is unloaded. In part II, the diode rectifier has been connected to the output, which is equal to the situation in Fig. 8. In parts III–XI, the adaptation to a circular output voltage can be followed. Part XII is after an additional ten adaptations and equals the situation in Fig. 9. The output voltage vector is now again sinusoidal as in part I, while the controller voltage compensates for the load.

A second experiment with unbalanced linear load is performed. An inductive load of 5 kVA is connected between two phases. The third phase is left unloaded. In Fig. 11, the inverter reference and the resulting output voltage trajectory is shown before compensation and, in Fig. 12, after compensation.

The small deviations in Fig. 12 from a circle on the sides contain frequency components that are above the FIR filter cutoff frequency and close to the resonance frequency of the output filter. These frequencies are not available in the feedback signal after the FIR filtering and the controller is, therefore, not able to compensate for these deviations, however, the output voltage has a high quality.

VII. CONCLUSION

In this paper, a high-performance control strategy for UPS systems was described that is able to compensate for distortion and unbalance generated by nonlinear and unbalanced loads or by nonlinearity in the inverter.

The principle can also be used in any static power supply system like power supplies and ground power units.

The DSP-controlled UPS system adapts the inverter reference to achieve sinusoidal balanced output voltages at nonlinear and nonsymmetrical loads by comparing the vectorial output voltages with a circular reference in fixed points on the fundamental period. Noncontrollable frequencies are avoided in the integrating control loop by an FIR filter that suppresses frequencies around and above the output filter resonance frequency.

The implementation of this control strategy on different systems is eased by the low dependency of the output filter parameters. The performance was verified on a 10-kVA system.

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